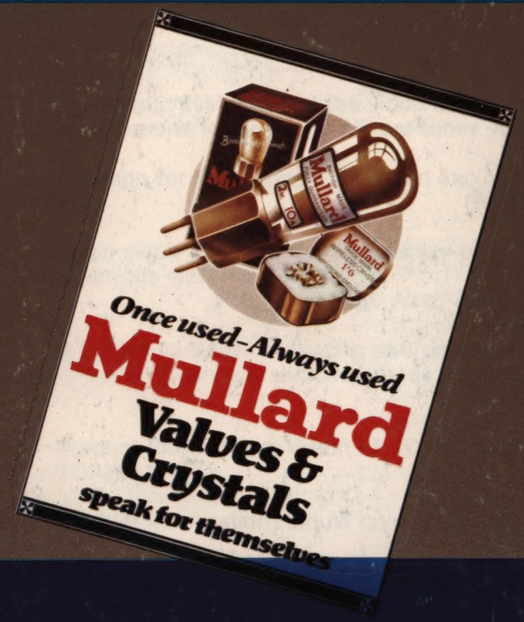
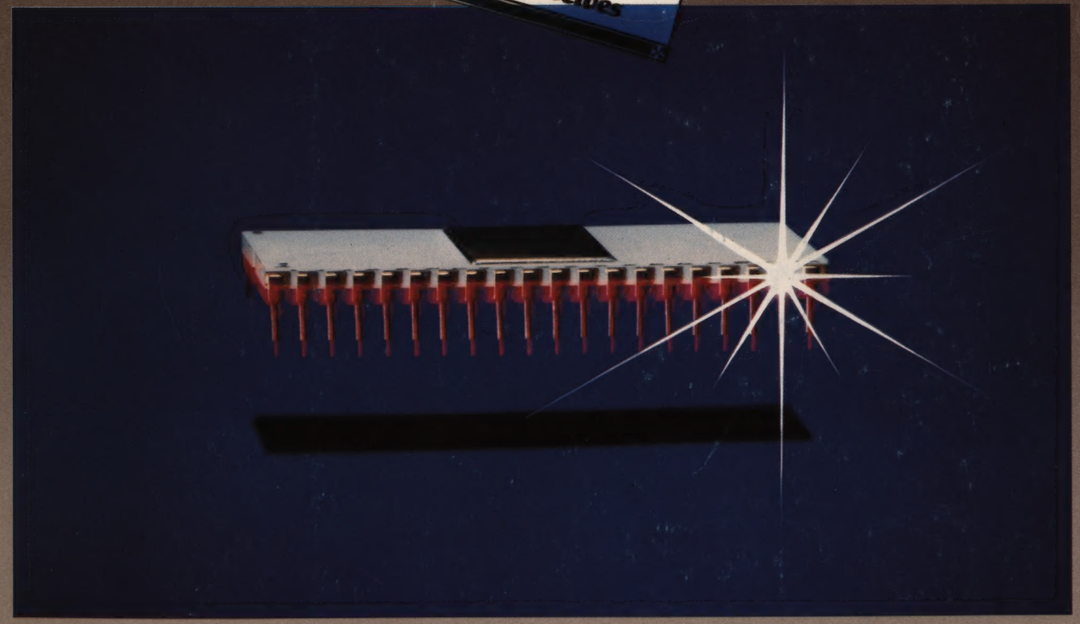
Mullard

Technical Communications

Volume 14 Number 140 October 1978





- Systematic evaluation of the video drive requirements for colour tv picture tubes
- A design for the display logic of an inexpensive VDU
- Radio clock for reception and display of MSF time-code transmission
- A sample-and-hold balancing and protection circuit for push-pull switched-mode power supplies
- Vision-i.f. ICs TDA2540 and TDA2541
- Liquid crystal displays

Mullard Technical Communications

ISSN 0027—3139

Volume 14 Number 140 October 1978

Systematic evaluation of the video drive requirements for colour tv picture tubes *A. Ciuciura* 379

A design for the display logic of an inexpensive VDU *H. M. Farmer* 392

Radio clock for reception and display of MSF time-code transmission *P.G. Giles, P.J. Hart, and I. Thomas* 402

A sample-and-hold balancing and protection circuit for push-pull switched-mode power supplies *L.E. Jansson* 424

Product Information: Vision-i.f. ICs TDA2540 and TDA2541 439

Product Information: Liquid crystal displays 442

Cover picture:

The cover represents two revolutions in the electronics industry. At the top, the pre-war advertisement illustrates the rapid expansion of 'wireless' in the late 1920s and early 1930s – an expansion helped by Mullard valves and components. Below it is the 2650 microprocessor. The microprocessor is the latest product of solid-state technology, and the full consequences of its introduction have yet to be seen.

Editor:
Edmund G. Evans

Assistant Editor:
Michael J. Prescott

Design and Production:
Michael J. Rose

Technical Publications Department
Mullard Limited,
New Road, Mitcham,
Surrey, CR4 4XY

Made and Printed in England by
The Yale Press Ltd.,
Carmichael Road, London, S.E.25.

© Mullard Limited 1978

This journal records developments in the application of electronics in science, industry, and the home. It contains information on the properties and performance of solid-state devices, valves and tubes, and associated components and assemblies. The practical circuits given are designed to provide the best working conditions and performance for the devices used. The design principles may be used (so far as device ratings allow) for adaptation to meet particular requirements. Current data should be consulted before any circuit is considered for production. Mullard Limited can normally supply only those devices or assemblies listed in the Company's current catalogues. Availability in quantity should be confirmed.

All information is published in good faith, but because of the wide variety of situations in which this information may be used, we cannot accept any responsibility for loss or damage resulting from unsatisfactory performance. Publication of this information does not imply any authority or licence for the utilisation of any patented feature.

Four issues are published each year and issued free of charge to equipment designers, research organisations, laboratories, libraries, educational establishments, and consultants. Requests for addition to the mailing list must be made on the official stationery of the establishment concerned.

Technical enquiries should be addressed to the Editor. Abstracts or references should mention both source and authors. Requests for republication or translation should be made to the Editor in writing.

'Mullard' is the trade mark of Mullard Limited and is registered in most of the principal countries of the world.

Mullard manufacture and market electronic components under the **Mullard, Philips,** and **Signetics** brands.

Mullard Limited, Mullard House, Torrington Place, London WC1E 7HD Tel: 01-580 6633 Telex: 264341

Editorial

This, the 140th issue of Mullard Technical Communications, is the last, after twenty-six years of regular publication. Why, our readers may well ask, should a journal that clearly might have continued indefinitely suddenly be replaced? The answer to that question lies in what is deemed appropriate at any particular time.

The years when Mullard Technical Communications was planned, launched, and first used as a carrier of technical information were those years when the entire electronics industry was blossoming at an unprecedented rate. Multitudes of circuit-designers and equipment-designers in myriad electronic companies were hungry for all of the applications information that Mullard engineers could provide, and contacts established through this information-flow have been beneficial to both sides.

The years that we are passing through now, a quarter of a century later, have given us a background of increased technological complexity, a readership consisting of more specialised circuit-designers, and a new sensitivity about the ability of the electronics industry to continue growth unabated. A changed strategy is required to ensure the most effective interaction between Mullard, as a components manufacturer and supplier, and our readers and customers.

Gradual changes within our own organisation have taken place in the same quarter of a century, and Mullard now operates increasingly as part of the international Philips organisation, to everyones' advantage.

Now, twenty-six years after the first edition of Mullard Technical Communications, there exists the possibility of improving the methods of communicating technical information to our readers. A journal which is more appropriate for the 1980s can be, and has been, devised, and our own internal methods of producing that journal have also been improved.

The new journal, Electronic Components and Applications, will provide a broader view of our total capability in electronic components, while still meeting the needs of our readers for technical information.

Edmund G. Evans Editor

Systematic evaluation of the video drive requirements for colour tv picture tubes

A. CIUCIURA
Mullard Application Laboratory

A systematic and straightforward method of determining the video drive requirements for tv picture tubes is described. To illustrate the method, the particular requirements of RGB cathode drive for the 20AX family of tubes are evaluated.

INTRODUCTION

The task of manufacturing colour television receivers capable of a high standard of colour reproduction is made easier by the high quality of modern colour picture tubes. However, to realise this high standard in all the receivers produced, the designer must allow for spreads in the tube characteristics. For example, allowance needs to be made for the spread in video drive requirements, since the magnitude of the video drive affects the light output and spot quality. Unfortunately little information has been published to date on the range of video drive requirements for colour picture tubes. Therefore, to assist the designer, this article describes a tried-and-tested method for determining the exact range of video drive requirements taking 20AX tubes as examples. The designer can then confidently predict that all receivers will perform satisfactorily (at least as far as video drive is concerned). The method describes the particular case of RGB cathode drive, but information on grid drive and unitised gun operation is also included.

METHOD OF APPROACH

One objective of television receiver design is to ensure that all the receivers produced meet the manufacturer's specification, allowing for the normal production spreads in the components used. This article uses the known tolerances on the characteristics of 20AX tubes as examples to determine the worst-case video drive requirements. The limiting value of the long-term average beam current (taken from the published data) and the normal programme signal levels are used to establish a target value for the total peak beam current. Then, account is taken of the tolerances of the characteristics of the tubes (in particular, the spreads in perveance, penetration, and current ratios of the guns). By combining the target beam current value with these tolerances, a hypothetical worst-case beam current for each colour is calculated. In turn, this permits the calculation of worst-case video drive values, using the published data. To establish the limiting values of the video amplifier outputs, a further calculation is made to take account of the resistors in series with the cathodes.

The choice of cut-off voltage for a picture tube determines the peak beam current available; in turn, the cut-off voltage is governed by the voltage on the second grid (the second grid is sometimes identified as the first anode). The normal mode of operation of a 20AX tube (and similar tubes) is with identical cut-off voltages for the three guns but with different second-grid voltages. Therefore, in this article, this is the mode of operation given most consideration in determining the video amplifier output requirements. However, some notes are included on the operation of picture tubes with the three second grids connected together.

PEAK BEAM CURRENT

The limiting value of the total long-term average beam current is 1.0mA in any of the 20AX family of tubes. However, this limit may be raised to 1.5mA if a beam

current limiting circuit is used, on the valid assumption that, in normal service, the tube only occasionally reaches the limiting value of 1.5mA.

Measurements show that during normal television programmes the peak-to-mean beam current ratio in the picture tube is about 10:1, and seldom falls below 5:1. It is felt that, since the current ratio of 5:1 is only exceeded for 5% of the viewing time, this ratio is a suitable basis for calculation. The visual disturbance caused by the limiting action during this 5% of the time should be minimal.

Therefore, on the basis of the above assumptions, the maximum total peak current is 7.5mA (five times the maximum total long-term average current). The division of this current between the three electron guns is determined by the reference white chosen and the tolerances of the characteristics of the picture tube, as discussed in the following section.

TOLERANCE OF PEAK BEAM CURRENT VALUES

To produce a picture white of a specified chromaticity, the red, green, and blue phosphors of a colour picture tube must be excited by beam currents in defined proportions. The required beam current ratios and their tolerances are published by the tube manufacturers, often giving ratios for more than one white. Table 1 gives the anode current ratios that are applicable to any of the 20AX family of tubes. (Other tubes with similar phosphors will have similar current ratios.)

The relationship between the beam current and the light output is linear over the range of beam currents encountered in television applications. It is therefore possible to evaluate the expected beam currents in the red, blue, and green guns, given the total beam current and the ratios of the individual beam currents to one another. The following calculations are carried out for illuminant D_{6500}, because this is the reference white adopted for colour television in Europe.

Consider the following average conditions:

ratio of red-to-green current = 1.30,

ratio of red-to-blue current = 1.55.

Assuming that the red gun is set at 1mA:

red current i_R = 1.00mA

green current i_G = 0.77mA (1.00mA ÷ R/G)

blue current i_B = 0.65mA (1.00mA ÷ R/B)

Total 2.42mA

However, the total peak beam current has previously been determined as 7.5mA. Therefore, multiplying the above values by 7.5/2.42 gives:

red current i_R = 3.11mA

green current i_G = 2.39mA

blue current i_B = 2.00mA

total 7.50mA as required.

Similar calculations can be performed for all possible combinations of ratios (maximum, minimum, and average) and the results are given in Table 2.

Each column in Table 2 represents a possible combination of beam currents that can occur in a 20AX picture tube which is producing illuminant D_{6500}. The figures specify particular situations, but in practice there is a continuous range of values, though some values will occur more frequently than others. Therefore the population of picture tubes has three simultaneously variable parameters which are interdependent.

TABLE 1

Anode Current Ratios in 20AX Tubes

		To produce white of the following CIE coordinates		
	x	0.265	0.281	0.313 *
	y	0.290	0.311	0.329 *
Ratio of anode currents red gun to green gun	min	0.60	0.65	0.95
	av	0.75	0.85	1.30
	max	1.00	1.15	1.70
Ratio of anode currents red gun to blue gun	min	0.50	0.65	1.15
	av	0.65	0.90	1.55
	max	0.90	1.20	2.05

*Illuminant D_{6500}

TABLE 2

Possible Values of Beam Currents Resulting from the Tolerances in Current Ratios

i_R/i_G		0.95			1.30			1.70		
i_R/i_B		1.15	1.55	2.05	1.15	1.55 (nominal tube)	2.05	1.15	1.55	2.05
Red current	(mA)	*2.57*	2.78	2.95	2.84	3.11	3.32	3.05	3.36	*3.61*
Green current	(mA)	2.70	2.93	*3.11*	2.19	2.39	2.56	*1.79*	1.98	2.12
Blue current	(mA)	2.23	1.79	*1.44*	2.47	2.00	1.62	*2.65*	2.17	1.76

i_{tot} = 7.5mA, Illuminant D_{6500}

Note: figures in italic are max and min values

It is difficult to describe mathematically such a population. A better approach is to consider three separate populations of red, green, and blue guns, rather than a single population of picture tubes. These are not exactly equivalent approaches, but produce similar results. Therefore, Table 2 shows that the range of currents in the three guns is:

i_R = 3.11 (+16%, −17%) mA,

i_G = 2.39 (+30%, −25%) mA,

i_B = 2.00 (+32%, −28%) mA.

DERIVATION OF HYPOTHETICAL BEAM CURRENTS

The range of beam currents given above can be combined with the published cathode drive characteristics to give a range of video drive voltages. However, the characteristics are published for nominal tubes only; to obtain the overall range of video drive voltages it is necessary to return to the basic concepts of the operation of an electron gun.

The relationship between the beam current and video drive voltage is not simple (see Eq.6 in the Appendix), and depends on the perveance and penetration (see the following section for an explanation of these terms) of the electron gun. Perveance and penetration are subject to manufacturing tolerances, so that there are three independent tolerances (beam current ratios, perveance, and penetration) contributing to the overall spread in video drive requirements. The combination of these three tolerances to determine the spread of video drive voltages can be achieved in several ways. The method adopted in this article is to convert all the tolerances to hypothetical beam current tolerances and to derive the required video drive voltages from these hypothetical currents. Using this method, the conversion from beam current to drive voltage is made once only, resulting in a comparatively simple calculation.

Effect of perveance and penetration

Eq.6 in the Appendix shows that the beam current i_b for cathode drive is given by:

$$i_b = \frac{k\left\{(1+D)\,v_{dk}\right\}^3}{(V_c + D\,v_{dk})^{3/2}},$$

where v_{dk} is the video drive voltage, V_c is the spot cut-off voltage, k is the perveance (or quality factor) of the cathode, and D is the penetration.

Perveance is a measure of the emission of the electron gun and has a value of $3\mu A/V^{3/2}$ for 20AX tubes (and has a similar value for other colour picture tubes). The variation in this value is significantly asymmetric, being +3%, −13%.

Penetration is the slope of a graph of spot cut-off voltage against second-grid voltage. Such a graph is included in the 20AX published data, for example, as the 'spot cut-off design chart (grid drive)'. Eq.6 shows that the relationship between i_b and D is complex, depending on the ratio v_{dk}/V_c. However, the picture tube is normally used under conditions that result in the ratio v_{dk}/V_c being near to unity, in which case i_b is proportional to $(1 + D)^{3/2}$. Therefore, it is easy to calculate the effect that variations in D will have on i_b. Examination of the published data for any of the 20AX tubes gives the values of D summarised in Table 3. Thus $(1 + D)^{3/2}$ = 1.48 (+9.2%, −8.4%) and this will result in a similar variation in i_b

TABLE 3

Variability of Penetration

	Penetration D	$(1 + D)^{3/2}$
D_{max}	$\frac{200 - 18}{480} = 0.379$	1.62
D_{av}	$\frac{200 - 16}{612} = 0.301$	1.48
D_{min}	$\frac{200 - 12}{830} = 0.227$	1.36

Addition of tolerances

The tolerances expressed in terms of beam current are:

all guns	+3% –13%	due to the perveance tolerance
	+9% –8%	due to the penetration tolerance
red gun	+16% –17%	due to the current ratio tolerance
green gun	+30% –25%	
blue gun	+32% –28%	

In view of the asymmetry of these distributions and the lack of knowledge of the shape of each distribution, it is reasonable to assume a Gaussian shape embracing the total population. This approach provides an extra margin of safety in the calculations.

The tolerances are not correlated and their resultant is therefore the root of the sum of the squares. Thus the tolerances for the three beam currents are given by:

$$S_{colour} = \sqrt{(S_k^2 + S_D^2 + S_R^2)},$$

where S_{colour} is the overall tolerance, S_k is the tolerance due to perveance, S_D is the tolerance due to penetration, and S_R is the tolerance due to current ratios. Therefore:

$$S_{red} = \sqrt{(13^2 + 9^2 + 17^2)},$$
$$= 23\%;$$
$$S_{green} = \sqrt{(13^2 + 9^2 + 30^2)},$$
$$= 34\%;$$
$$S_{blue} = \sqrt{(13^2 + 9^2 + 32^2)},$$
$$= 36\%.$$

TABLE 4

Overall Range of Hypothetical Beam Currents

	Peak current (mA)		
	max	av	min
Red current	3.82	3.11	2.39
Green current	3.20	2.39	1.58
Blue current	2.72	2.00	1.28

The tolerances are applied to the average beam currents (see Table 2, 'nominal tube') to determine the overall range of hypothetical beam currents given in Table 4. It is worth stressing that the range of currents in Table 4 is hypothetical; the range likely to be encountered in practice is given in Table 2.

VIDEO DRIVE

The following discussion considers only the case of video drive voltage applied to the cathodes of a picture tube, because this is the usual modern practice. Eq.6 in the Appendix is applicable to this type of drive and it shows the complexity of the relationship between the drive voltage and the beam current. It is possible to derive an implicit equation for the cathode drive voltage in terms of the beam current, but the equation is not simple and there may be significant differences between the theoretical and empirical values. Therefore it is preferable to use the published data, though quite often this is presented in too general a form to be useful. However, the published graphs can be redrawn using more convenient scales and adding extra curves by interpolation. Characteristics for 20AX tubes, produced in this way, are shown in Fig.1.

Fig.1 has a format similar to the published data, but it is possible to rearrange the same information in other ways; one way is shown in Fig.2. The main advantage of this presentation is that the change in video drive voltage as a function of cut-off voltage, for a particular beam current, is immediately visible. (The beam current values used in Fig.2 are taken from Table 4.)

Cut-off voltage

When selecting a cut-off voltage as part of the design procedure of a tv receiver, it is necessary to ensure that the required peak beam currents can be obtained before the guns are driven into the region of grid current (reference to Fig.2 shows that a minimum value of 95V would suffice in the case under consideration). However,

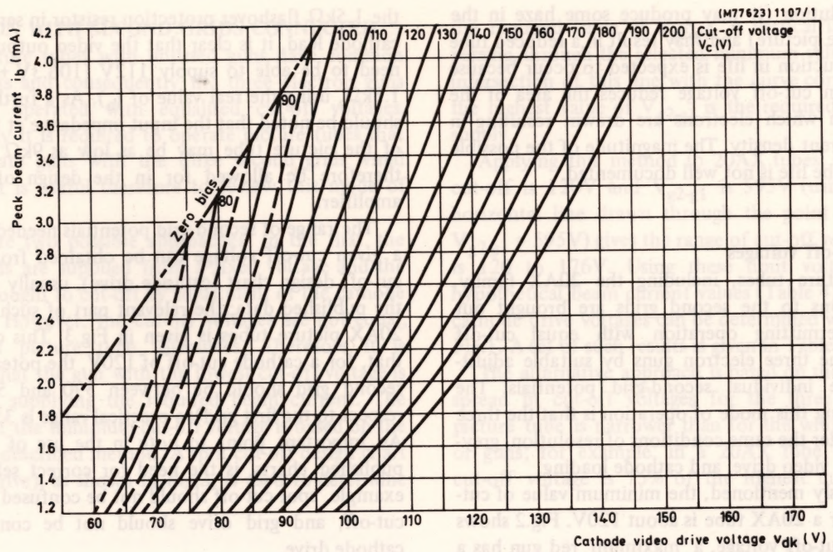


Fig.1 — Cathode drive chart

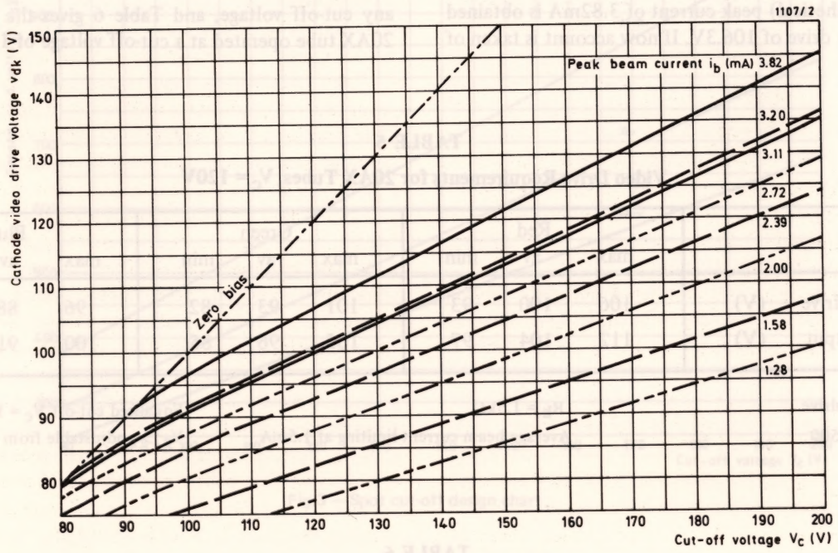


Fig.2 — Drive chart for specific currents

it is good practice to allow a margin of about 15V between the zero-bias voltage and the maximum expected drive voltage, because this region of the characteristic is associated with distortions of the electron beam, resulting in a noticeably worse definition. Also, the γ (see Appendix for definition) of the electron gun can change in this region, leading to a possible deficiency in grey-scale tracking. Thus inspection of Fig.2 shows that a suitable minimum cut-off voltage is 120V (giving 13V 'headroom' for the worst-case tube).

The choice of whether or not to increase the cut-off voltage above this minimum is subject to conflicting requirements. A moderate increase in the cut-off voltage may produce an improvement in resolution, but will require an increase in video drive voltage (as may be seen from Fig.2). A further increase in cut-off voltage will not

improve resolution (it may produce some haze in the corners of the picture) and may result in a reduced tube life. This reduction in life is expected to occur because an increase in cut-off voltage reduces the area of the cathode from which electrons are drawn, resulting in increased current density. The magnitude of the possible decrease in tube life is not well documented.

Equalised cut-off voltages

In many picture tubes, including the 20AX family, the connections to the second grids are brought out separately, permitting operation with equal cut-off voltages on the three electron guns by suitable adjustments to the individual second-grid potentials. The reason for using this mode of operation is that the three guns work under the same conditions of resolution, grey-scale tracking, video drive, and cathode loading.

As previously mentioned, the minimum value of cut-off voltage for a 20AX tube is about 120V. Fig.2 shows that, at this cut-off voltage, a 'maximum' red gun has a reserve of 13V before the zero-bias state is reached and a 'nominal' red gun has a reserve of 20V. Thus, the maximum (hypothetical) peak current of 3.82mA is obtained with a video drive of 106.3V. If now account is taken of the 1.5kΩ flashover protection resistor in series with the cathode lead, it is clear that the video output stage will need to be able to supply 112V (106.3V + 3.61mA × 1.5kΩ, using the real value of i_b). As a further point, it should be noted that the input impedance at the cathode of the picture tube may be as low as 9kΩ and should therefore be allowed for in the design of the video amplifier.

The range of second-grid potentials needed to provide a given cut-off voltage can be obtained from the spot cut-off design chart (cathode drive), usually included in the published data; the relevant part of such a chart for 20AX picture tubes is given in Fig.3. This chart shows that, for a cathode cut-off of 120V, the potential on the second grid should be between 390 and 595V (with respect to the first grid); a practical range is 350 to 650V. An important point to note in the use of any of the published charts, is the need for correct selection; for example, spot cut-off should not be confused with raster cut-off, and grid drive should not be confused with cathode drive.

The results of the preceding calculations are summarised in Table 5. Similar tables can be constructed for any cut-off voltage, and Table 6 gives the results for a 20AX tube operated at a cut-off voltage of 145V.

TABLE 5

Video Drive Requirements for 20AX Tubes, V_c = 120V

		Red			Green			Blue		
		max	av	min	max	av	min	max	av	min
Cathode drive	(V)	106	100	93	101	93	82	96	88	76
Video output	(V)	112	104	97	105	96	85	100	91	78

RGB cathode drive
Illuminant D_{6500}
R_k = 1.5kΩ
Average beam current limiting at 1.5mA
Equalised cut-off V_c = 120V
$V_{g2\text{-}g1}$ adjustable from 390 to 595V

TABLE 6

Video Drive Requirements for 20AX Tubes, V_c = 145V

		Red			Green			Blue		
		max	av	min	max	av	min	max	av	min
Cathode drive	(V)	119	111	103	112	103	90	107	97	84
Video output	(V)	124	116	107	117	106	93	111	100	86

RGB cathode drive
Illuminant D_{6500}
R_k = 1.5kΩ
Average beam current limiting at 1.5mA
Equalised cut-off V_c = 145V
$V_{g2\text{-}g1}$ adjustable from 470 to 730V

OPERATION WITH SECOND GRIDS CONNECTED

Colour picture tubes with unitised guns have common second grids and consequently the three electron guns cannot be operated with equalised cut-off voltages. Occasionally it is required to operate picture tubes that have separate guns with the three second grids wired together; it is useful therefore to review this mode of operation.

There are two possible approaches. In the first, the second grids are supplied from a fixed voltage and the guns are brought to cut-off by adjustment of the cathode potentials. However, the cut-off voltages are not equal, because of picture tube tolerances. Therefore it is necessary that the gun with the lowest cut-off voltage is capable of supplying the required beam current. The selection of the minimum cut-off voltage is based on the previously described method. A spot cut-off design chart (cathode drive), as shown in Fig.3, is used to determine the required value of $V_{g2\text{-}g1}$. A vertical line is drawn, passing through the selected minimum value of V_c: the intersection of this line with the curve corresponding to the highest value of $V_{g2\text{-}g1}$ is the required value of the supply.

Applying this method to 20AX tubes, the minimum cut-off is 120V and $V_{g2\text{-}g1}$ is 595V (using Fig.3). A horizontal line drawn through the point (V_c = 120V, $V_{g2\text{-}g1}$ = 595V) gives the range of cut-off voltages, which is 120 to 176V. Using these limit voltages and the hypothetical beam current values (Table 4), the range of cathode drive voltages can be determined with the aid of Fig.1. A set of such results is given in Table 7.

The alternative approach is based on the fact that the spread in cut-off voltages for the three guns in one picture tube is narrower than for the whole population of guns; for example, in a 20AX tube the minimum cut-off voltage is 75% of the highest cut-off voltage.

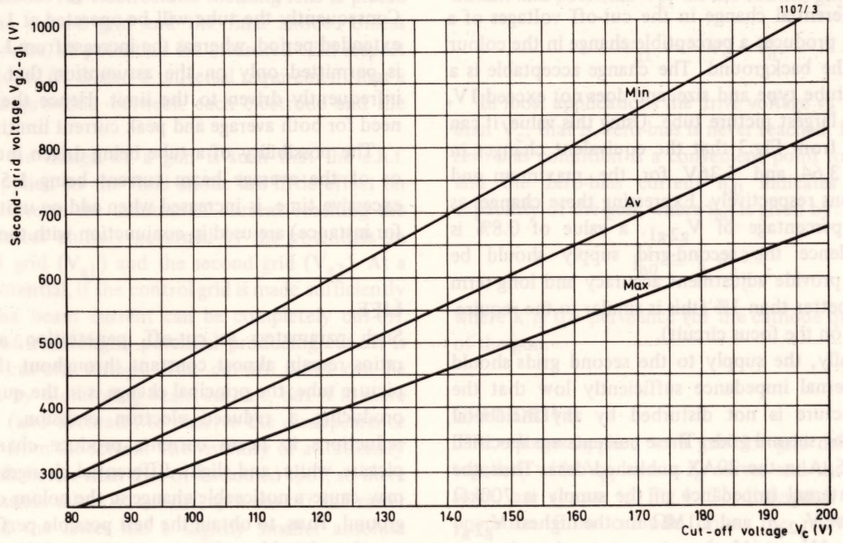


Fig.3 — Spot cut-off design chart

TABLE 7

Video Drive Requirements with Second Grids Connected, $V_{g2\text{-}g1}$ Fixed

		Red	Green	Blue
Cathode drive	(V)	93 to 133	82 to 126	76 to 120
Video output	(V)	97 to 139	85 to 130	78 to 124

RGB cathode drive
Illuminant D_{6500}
R_k = 1.5kΩ
Average beam current limiting at 1.5mA
V_c adjustable in the range 120 to 176.5V
$V_{g2\text{-}g1}$ fixed at 595V

Thus, if a V_c of 120V is selected as a minimum value, the maximum is 160V (120 × 100/75); by comparison the corresponding spread for the whole population is 120 to 176V. Consequently, by adjusting $V_{g2\text{-}g1}$, the spread of cut-off voltages in a television receiver can be reduced. Thus it is possible to stipulate a minimum cut-off of 120V (for example) for each tube and to adjust the voltages on the other two cathodes to bring them to cut-off. The minimum cut-off is achieved by adjusting $V_{g2\text{-}g1}$. The overall result of this procedure is a considerable shift of the whole population of cut-off voltages towards the optimum value. It can be seen that, for a 20AX tube operated in this mode, the range of cut-off voltages is 120 to 160V and $V_{g2\text{-}g1}$ must be adjustable between 390 and 595V. The range of cathode drive voltages and the required outputs from video amplifiers are listed in Table 8.

STABILITY OF SECOND-GRID VOLTAGE

A small differential change in the cut-off voltages of a picture tube produces a perceptible change in the colour balance of the background. The change acceptable is a function of tube type and size, and does not exceed 1V, even for the largest picture tube. Using this value, it can be deduced from Fig.3 that the equivalent changes in $V_{g2\text{-}g1}$ are 3.64 and 5.36V for the maximum and minimum guns respectively. Expressing these changes as an average percentage of $V_{g2\text{-}g1}$, a value of 0.8% is obtained. Hence the second-grid supply should be designed to provide adjustment accuracy and long-term stability of better than 1% (this is similar to the requirement placed on the focus circuit).

Additionally, the supply to the second grids should have an internal impedance sufficiently low that the displayed picture is not disturbed by any incidental currents in the second grids. These currents are specified as less than 5μA in the 20AX published data. Thus, the maximum internal impedance of the supply is 700kΩ for the lowest $V_{g2\text{-}g1}$, and 1.1MΩ for the highest $V_{g2\text{-}g1}$ (impedance = $\Delta V_{g2\text{-}g1}/\Delta I_{g2}$).

BEAM CURRENT LIMITING

As previously mentioned, the limiting value of the total long-term average beam current is 1mA in a 20AX tube, but 1.5mA is permitted provided that a current limiting circuit is used. This increase is on the assumption that a picture tube is only occasionally driven to the limit.

However, if the current sensing circuit operates only on average values, some complications may arise. For example, in a receiver with abundant video drive and a contrast control accessible to the viewer, it is possible that during high peak-to-mean ratio pictures (night scenes) the contrast control may be adjusted so that the picture tube is almost driven into zero-bias conditions, but the average beam current will be well below 1.5mA. Therefore, the picture will suffer from increased spot size and poor resolution due to operation close to the zero-bias region. If the picture then changes to give a more normal peak-to-mean ratio, and the contrast control is not readjusted, then the average limiting circuit will try to maintain an average current of 1.5mA. Consequently the tube will be operated at 1.5mA for an extended period, whereas the increase from 1.0 to 1.5mA is permitted only on the assumption that the tube is infrequently driven to the limit. Hence there is a clear need for both average and peak current limiting.

The possibility of a tube being driven into zero-bias, or of the average beam current being 1.5mA for an excessive time, is increased when add-on units (tv games, for instance) are used in conjunction with the receiver.

LIFE

Such parameters as cut-off, penetration, and current ratios remain almost constant throughout the life of a picture tube; the principal change is in the quality factor, producing a reduced electron emission. Differential reductions in beam currents produce changes in the picture white, and slight differential changes in cut-offs may cause a noticeable change in the colour of the background. Thus, to obtain the best possible performance, it may be advisable either to examine and, if necessary, to adjust the colour point at about yearly intervals, or to include an automatic correction circuit in the receiver.

It is sometimes argued that extra drive should be provided to allow for the fall in emission with age of a picture tube. The method described in this article ensures that every new tube is fully driven. This implies that the majority of tubes do have a margin of drive available. Additionally, an increased margin of drive is available because of the assumed Gaussian population distribution. The approach described in this article has been used over a long period and practical results indicate an entirely satisfactory performance with age.

TABLE 8

Video Drive Requirements with Second Grids Connected, $V_{g2\text{-}g1}$ Variable

		Red	Green	Blue
Cathode drive	(V)	93 to 126	82 to 119	76 to 113
Video output	(V)	97 to 131	85 to 123	78 to 117

RGB cathode drive
Illuminant D_{6500}
R_k = 1.5kΩ

Average beam current limiting at 1.5mA
Cathode cut-off voltage { minimum gun 120V; other guns 120 to 160V
$V_{g2\text{-}g1}$ adjustable from 390 to 595V

APPENDIX

Grid Drive and Cathode Drive Characteristics of a Picture Tube

ELECTRON GUNS

Although a modern colour picture tube has three electron guns, for the sake of simplicity the behaviour of only one gun is considered in this Appendix. Each gun is of tetrode construction; that is, it consists of a cathode, control grid, accelerating anode (second grid), and final anode. An electrostatic focusing lens is placed between the second grid and the final anode. Unless stated otherwise, all potentials are measured with respect to the cathode. (It is also a universal requirement that a d.c. path is provided between each electrode and the cathode.)

Usually the design of a gun is such that the e.h.t. potential applied to the final anode has little effect on the beam current; the amount of current reaching the screen is almost entirely governed by the potentials on the control grid (V_{g1}) and the second grid (V_{g2}). At a given V_{g2} potential, if the control grid is made sufficiently negative, the beam current can be completely cut-off. The value of control-grid potential producing cut-off is called the cut-off voltage. The cut-off point can be determined by monitoring beam current, but it is more convenient (and accurate) to observe the disappearance of the spot from the screen. The visibility of a stationary spot is much better than that of a scanned spot, so there are two possible values of cut-off, spot cut-off and raster cut-off, and the latter has a slightly smaller absolute value.

Normally, the published data provides a graph of the cut-off voltage as a function of V_{g2}; the graph includes the whole population of guns within the minimum and maximum lines. For any one gun, the relationship between cut-off and V_{g2} is linear and can be represented by the following equation:

$$V_c = a + D\,V_{g2}, \qquad \ldots(1)$$

where a is the intercept of the relevant straight line with the y-axis, D is the slope of the straight line ($= -\Delta V_{g1}/\Delta V_{g2}$), and V_c is the spot cut-off voltage. Typical values are a = −18 and D = 0.301 for an average A66-510X tube.

Absolute values of V_c and D are used to simplify the following calculations.

The receiver circuits are designed such that the cut-off voltage of a gun corresponds to the black level of the television signal and the gun is driven with a voltage v_d from the cut-off towards the zero-bias condition. At any instant the potential V_{g1} on the control grid is given by:

$$V_{g1} = -V_c + v_d. \qquad \ldots(2)$$

In most applications the drive voltage v_d is always less than V_c; that is, zero-bias is never reached. However, the zero-bias condition is a convenient point to assess a gun, and the zero-bias current i_{b0} indicates the current capability of the gun, where i_{b0} is given by:

$$i_{b0} = k\,V_c^{3/2}, \qquad \ldots(3)$$

where k is the perveance (or the cathode quality factor) of the gun.

GRID DRIVE

The voltages applied to a gun for grid drive operation, together with V_{g1} versus i_b curves and the video waveform, are shown in Fig.4. To distinguish this type of operation from cathode drive, the relevant voltages carry the subscript g or k respectively.

It should be noted that cathode potential V_k and

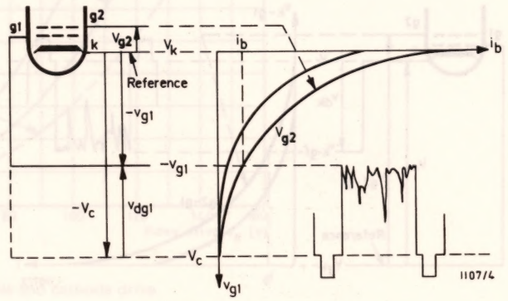


Fig.4 — Grid drive operation

second-grid potential V_{g2} remain fixed; the cut-off voltage V_c is determined by the magnitude of V_{g2} (Eq.1). The video drive v_{dg} is supplied to the control grid and so grid voltage varies as shown by Eq.2. The resulting beam current i_b as a function of video drive voltage is approximated by:

$$i_b = \frac{k}{V_c^{3/2}} v_{dg}^{3}. \quad \ldots(4)$$

When $v_{dg} = V_c$, that is when the gun control-grid voltage is zero, Eq.4 assumes the same form as Eq.3. Unfortunately, the reduction of Eq.4 to the form of Eq.3 does not necessarily indicate the validity of Eq.4; reference to the published data shows that Eq.3 is a good approximation to measured values, but the graphs for grid drive show some departure from the third power law of Eq.4.

CATHODE DRIVE

Cathode drive is universally employed in domestic television receivers because the video drive is reduced compared with grid drive. The voltage supplied to the gun, cathode voltage versus beam current characteristics, and the video waveform are shown in Fig.5. With the gun adjusted to cut-off, the voltages for cathode and grid drive are identical. However, in the case of cathode drive, V_{g2} and V_{g1} potentials are fixed and the signal is applied to the cathode. A negative-going video drive is necessary to produce an increase in current through the gun. Modulation on the cathode causes changes not only in V_{g1} but also in V_{g2}, in such a sense that both effects are additive, giving an increase in sensitivity.

This increase in sensitivity can be demonstrated mathematically in the following way. From Eq.1:

$$\frac{dV_c}{dV_{g2}} = D. \quad \ldots(5)$$

The application of video drive v_{dk} increases V_{g2} to

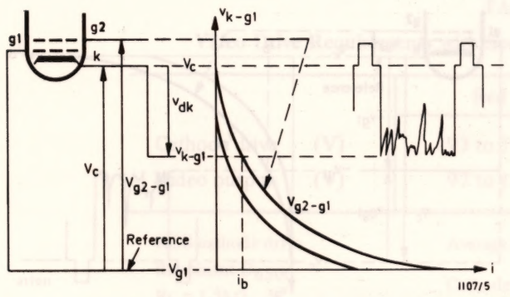


Fig.5 — Cathode drive operation

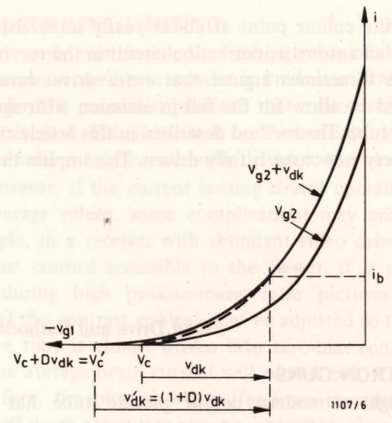


Fig.6 — Conversion from grid drive to cathode drive

$(V_{g2} + v_{dk})$. The resulting cut-off voltage is $V_c' = V_c + Dv_{dk}$ (from Eq.5). In terms of the grid drive characteristic, shown in Fig.6, the cathode drive moves the operating point from the original characteristic corresponding to V_{g2}, with a cut-off V_c, to a new characteristic $(V_{g2} + v_{dk})$, with a cut-off $V_c' = V_c + Dv_{dk}$. Now, at the same value of V_{g1}, a change in the cut-off voltage from V_c to V_c' is equal to a change in the drive voltage from the original v_{dk} to the new value v_{dk}' given by:

$$\begin{aligned} v_{dk}' &= V_c' - V_c + v_{dk}, \\ &= V_c + Dv_{dk} - V_c + v_{dk}, \\ &= (1 + D)\, v_{dk}. \end{aligned}$$

Substituting in Eq.4 the new value of cut-off voltage V_c' for V_c and the new value of drive voltage for v_d, the following equation applicable to cathode drive is obtained:

$$i_b = \frac{k}{(V_c + Dv_{dk})^{3/2}} \left\{(1 + D)\, v_{dk}\right\}^3. \quad \ldots(6a)$$

A more usual form of this equation is:

$$i_b = \frac{k\,(1 + D)^3\, v_{dk}^{3}}{\left(1 + D\dfrac{v_{dk}}{V_c}\right)^{3/2} V_c^{3/2}}. \quad \ldots(6b)$$

The practical maximum current i_{b0} is reached under zero-bias conditions; that is, when $v_{dk} = V_c$, in which case Eq.6 can be simplified to give:

$$i_{b0} = k\,(1 + D)^{3/2}\, V_c^{3/2}. \quad \ldots(7)$$

COMPARISON OF BEAM CURRENT VALUES

Comparison of Eq.3 with Eq.7 shows that the beam current for cathode drive is larger than that for grid drive by a factor $(1 + D)^{3/2}$, for the same cut-off voltage and at the zero-bias condition. With an average value of D = 0.301, this represents an increase of 48% in beam current. The same current could be obtained with grid drive if the cut-off voltage were increased by a factor (1 + D); that is, by 30%.

It is difficult to derive a simple, explicit equation for drive voltage from Eq.6; for this reason a comparison of v_d versus i_b characteristics for cathode and grid drive is shown in Fig.7. The curves in Fig.7 show the difference between grid drive and cathode drive characteristics for the same cut-off voltage (V_c = 120V), and a grid drive characteristic with cut-off (V_c = 156V) adjusted to give the same zero-bias current as for the cathode drive characteristic.

The amount of current a gun can deliver at zero-bias is an important aspect of its characteristic. In the selection of operating voltages, it is necessary to ensure that, for a given mode of drive, the cut-off voltage is large enough to provide the necessary current before the zero-bias condition is reached. Fig.8 shows graphs of zero-bias current against V_c for cathode drive and grid drive.

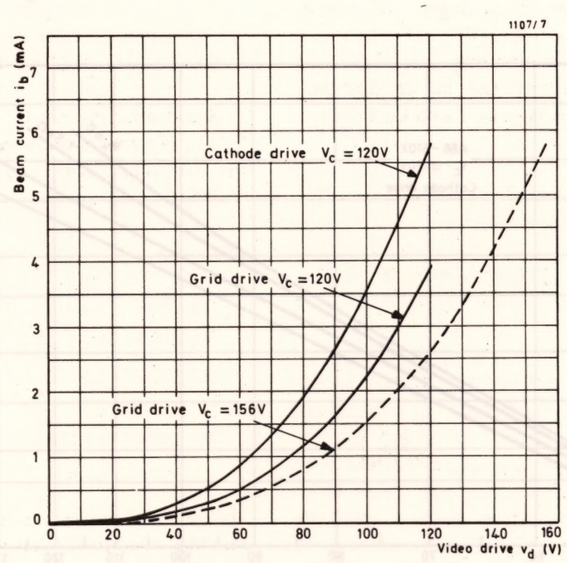


Fig.7 — Comparison of grid drive and cathode drive characteristics

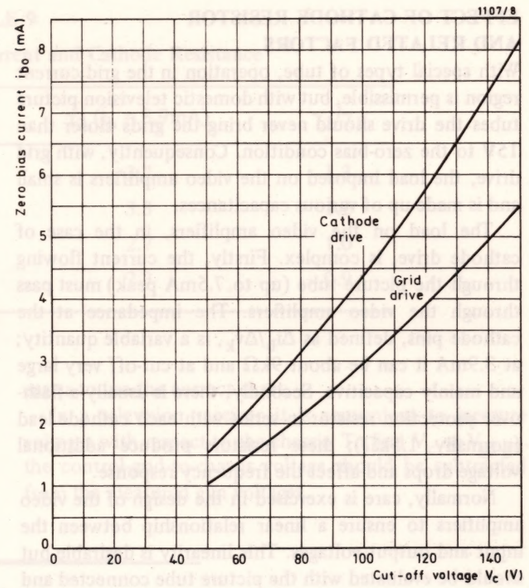


Fig.8 — Zero-bias current as a function of V_c for cathode drive and grid drive conditions

EFFECT OF CATHODE RESISTOR AND RELATED FACTORS

With special types of tube, operation in the grid current region is permissible, but with domestic television picture tubes the drive should never bring the grids closer than 15V to the zero-bias condition. Consequently, with grid drive, the load imposed on the video amplifiers is small and is made up of various capacitances.

The load on the video amplifiers, in the case of cathode drive, is complex. Firstly, the current flowing through the picture tube (up to 7.5mA peak) must pass through the video amplifiers. The impedance at the cathode pins, defined as $\Delta i_b/\Delta v_k$, is a variable quantity; at 3.9mA it can be about 9kΩ and at cut-off very large and mainly capacitive. Secondly, there is usually a flash-over protection resistor in series with each cathode lead (normally 1.5kΩ); these resistors produce additional voltage drops and affect the frequency response.

Normally, care is exercised in the design of the video amplifiers to ensure a linear relationship between the input and output voltages. This linearity is desirable but should be evaluated with the picture tube connected and properly driven, the output voltages being measured directly at the cathode pins.

Fig.9 shows the relationship between beam current and video amplifier voltage for several values of resistor in series with the cathode of a gun. It shows the increase in the required video drive, due to the presence of the resistor, and also illustrates the changes in the slope of the graph as a function of the value of the resistor. Since logarithmic scales are used, the slope is really the γ of the gun, where γ is given by:

$$\gamma = \frac{\log (I_1/I_2)}{\log (v_{dk1}/v_{dk2})}. \qquad \ldots (8)$$

In practice γ is a variable quantity, depending very much on the value of the cut-off voltage and proximity to the zero-bias region. However, for comparison, some values from Fig.9 are given in Table 9. The figures in Table 9 indicate a fall in the value of γ with increasing resistance; the fall is more pronounced at higher beam currents.

GRID AS REFERENCE

With cathode modulation, the cathode potential varies at video frequency and, therefore, the reference level is chosen to be the control-grid voltage. Apart from heater potential, the control-grid potential is the lowest voltage applied to a gun and, being constant, presents a convenient reference level. The cathode cut-off voltage is positive with respect to the control grid and the V_{g2} voltage is added to it. Thus:

$$V_{g2\text{-}g1} = V_{g2} + V_c. \qquad \ldots (9)$$

Often, the published data provides separate charts for grid and cathode cut-offs. However, numerically both cut-off voltages are the same, the only difference being

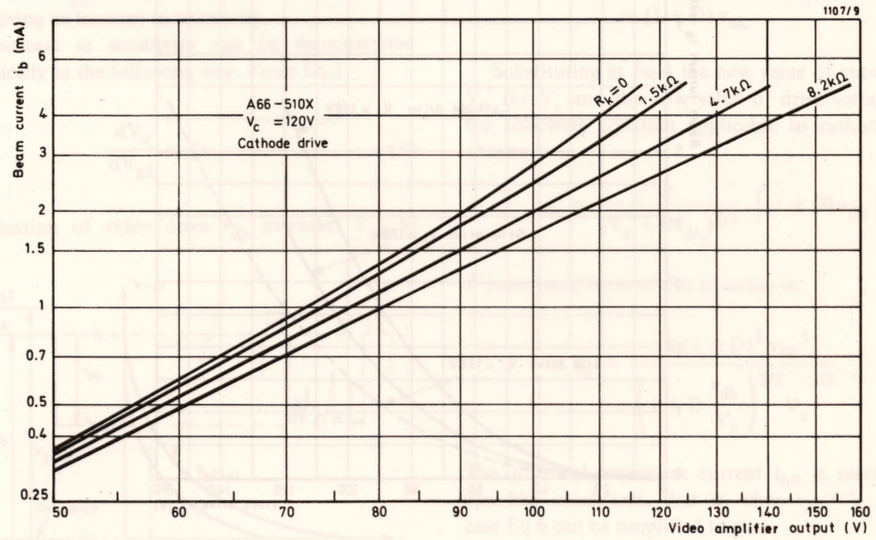


Fig.9 — Effect of cathode resistor on video amplifier output requirements

TABLE 9

Dependence of γ on Beam Current and Cathode Resistance

R_k (kΩ)	γ_1 (i_b = 1mA)	γ_2 (i_b = 3.9mA)	γ_2/γ_1
0	2.9	3.7	1.3
1.5	2.8	3.3	1.2
4.7	2.6	2.7	1.0
8.2	2.5	2.3	0.9

in the V_{g2} (for grid drive) and $V_{g2\text{-}g1}$ (cathode drive) scales. Given one of the charts, the other can be easily deduced using Eq.9. The conversion of a v_d versus i_b chart for grid drive to a chart for cathode drive, or vice versa, is a more complex procedure and it is therefore easier to use the correct chart.

In a television receiver it is convenient to measure voltages with respect to the chassis. To find V_c or $V_{g2\text{-}g1}$, the control-grid-to-chassis voltage should be subtracted from the measured gun voltages.

A design for the display logic of an inexpensive VDU

H.M. FARMER
Mullard Application Laboratory

This article describes the logic design of an inexpensive visual display unit (VDU). The logic circuit uses two LSI (Large-Scale Integration) circuits to perform the timing and character generation functions, thus reducing the number of additional integrated circuits and discrete components required. These LSI circuits were developed for the Mullard teletext data decoder, and thus many of the teletext display facilities are also available.

INTRODUCTION

In many applications the cathode ray tube is the only practical device which can be used to display large amounts of information, in spite of the recent advances in display technology. The visual display unit (VDU) has long been established as a computer peripheral, using specially designed logic circuits and professional tubes. However, in recent years the applications of VDUs have broadened extensively to include, for example, patient monitoring equipment and word processors. Consequently, a large potential market has developed for cheaper display devices.

A considerable cost reduction in the production of VDUs can be achieved by using mass-produced components designed to cover a wide range of applications. Television is one related application where the cost of existing high-quality components has already been reduced to a minimum through bulk use. The performance of modern television picture tubes is generally acceptable for the display section of VDUs with only 40 characters per row, such as office work stations and home computers, for instance. Additionally, the development of teletext information services (CEEFAX, ORACLE, and viewdata) has resulted in the development of integrated circuits which can provide many of the logic functions required in a VDU. Thus, by combining standard television tubes and teletext integrated circuits, a very economical VDU can be developed based on existing components.

Mullard has developed a complete range of LSI (Large-Scale Integration) circuits to realise a high-performance, yet economical, teletext data decoder (see Ref.1). This article describes how two of these LSI circuits can be used to provide the display logic of a passive VDU.

The display has the same format as a teletext display (that is, 24 rows of 40 characters per row) and many of the teletext facilities are available, such as graphics, double-height characters, and so on. While this logic circuit can form part of a colour system, it also provides an economical design for a monochrome display.

The Mullard teletext decoder contains four dedicated LSI integrated circuits and the main functions of these ICs are:

SAA5020	TIC	timing chain;
SAA5030	VIP	video input processor;
SAA5040	TAC	teletext data acquisition and control;
SAA5050	TROM	teletext read-only memory, the character generator.

Detailed consideration of the functions of these four ICs showed that two of the chips, TIC (SAA5020) and TROM (SAA5050), could form the basis of a circuit to provide the logic of a VDU.

The VDU based on the circuit described in this article has the following features.

1) 40 characters per row.
2) 12 or 24 rows per page, depending on character height.
3) Characters resolved on a 7-by-5 matrix, which is effectively increased to a resolution of 14-by-10 by character rounding*.
4) Monochrome or colour display.
5) Storage of a full page (40-by-24 characters) in the memory allows the equipment to operate independently during display.
6) Availability of full cursor control and many of the teletext facilities.
7) Few components, no adjustments, and a single 5V supply rail (supplying 800mA).

THE LOGIC CIRCUIT

Fig.1 shows a simplified block diagram of the logic circuit (with the cursor section omitted). The circuit can conveniently be divided into four sections which are discussed in turn below:

1) the timing chain,
2) the memory addresser (comprising the multiplexer/counter and address converter),
3) the display memory,
4) the character generator.

The timing chain TIC controls the major timing functions in the system from a 6MHz clock input (see Fig.1). During the display period it provides memory read signals for the column addresses and 5-bit row addresses. TIC also generates a Data Entry Window DEW for the external control equipment which defines the time during which data is entered into the page memory.

The memory read addresses and the address instructions (generated externally) are passed to the address converter by the multiplexer/counter. The address converter converts the 5 bits of row address and 6 bits of column address to a 10-bit memory address.

The memory itself stores the 7-bit teletext codes for the display and control characters, and supplies a 7-bit character code to the character generator TROM. TROM provides the required video drive signals for the display in response to timing signals from TIC and character data from the memory. If required, an internally-generated sync signal is available from TIC.

Fig.2 shows a complete diagram of the logic circuit, and Fig.3 is a picture of a typical home terminal which could be used with the logic unit discussed here.

Timing chain TIC (SAA5020)

The timing chain TIC (IC_1 in Fig.2) is an MOS n-channel IC which has been developed to perform the timing functions for a teletext system. The principal input is a 6MHz clock signal; the divider stages in TIC subdivide

*UK Patent Nos.1343298 and 1515506

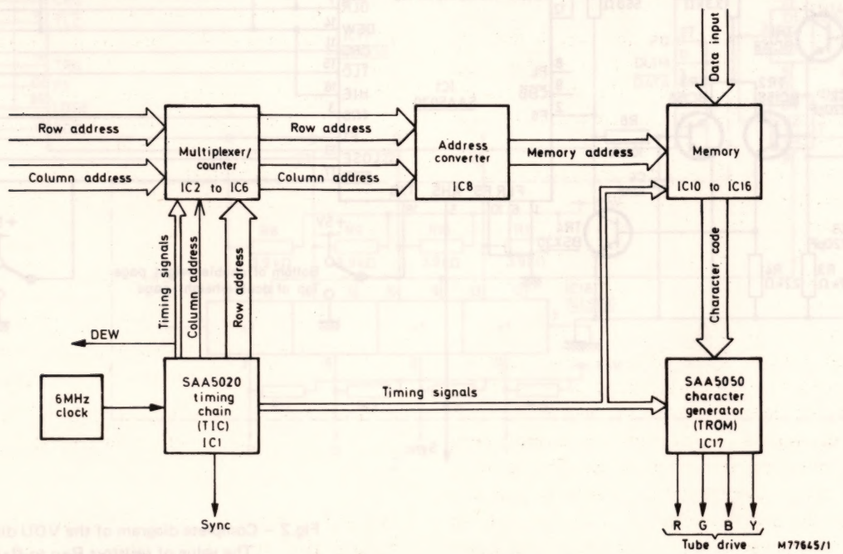


Fig.1 – Block diagram of the VDU display logic circuit (with the cursor section omitted)
The IC numbers refer to Fig.2

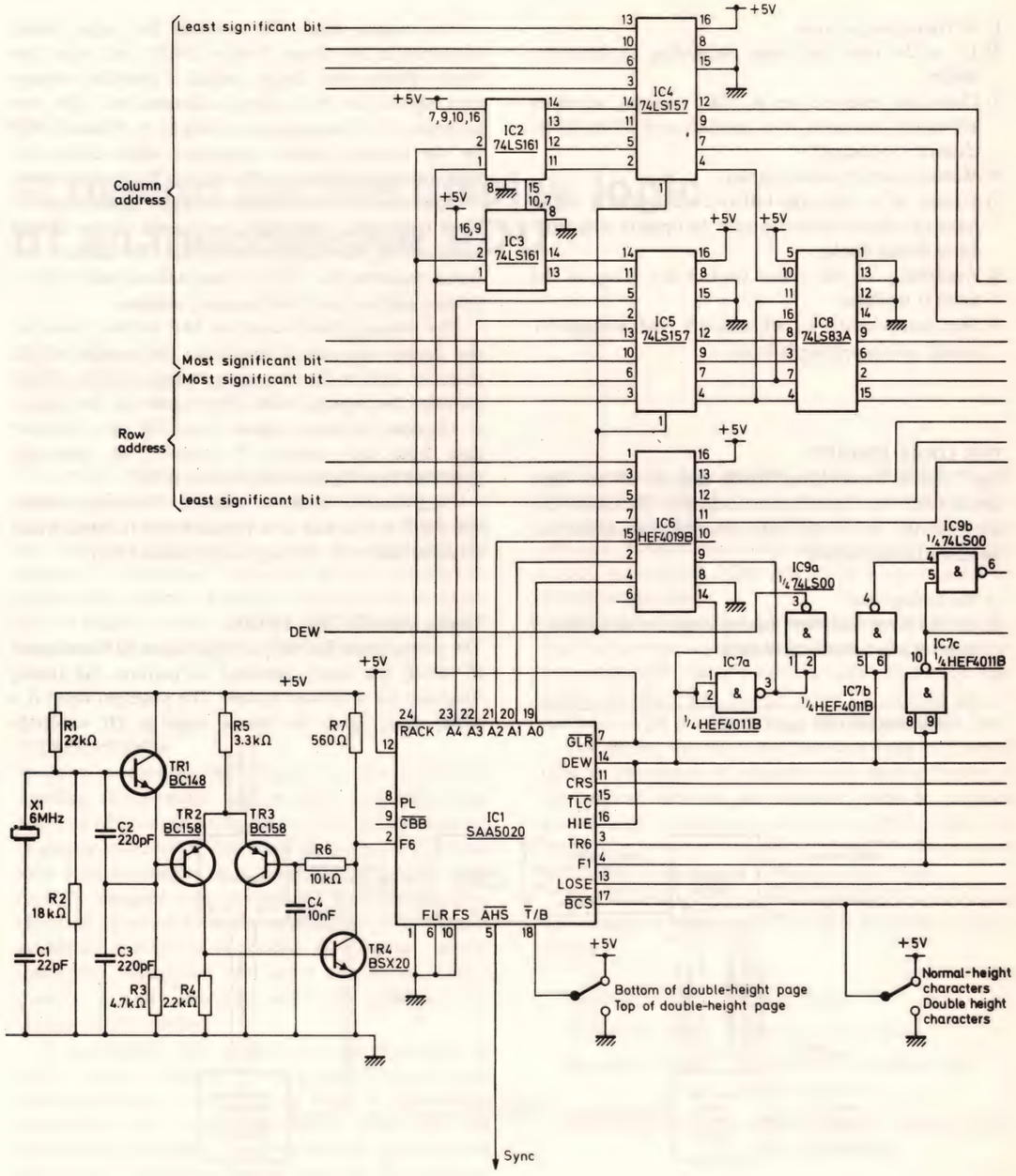


Fig.2 — Complete diagram of the VDU display logic. The value of resistors R_{12} to R_{15} depends on the application

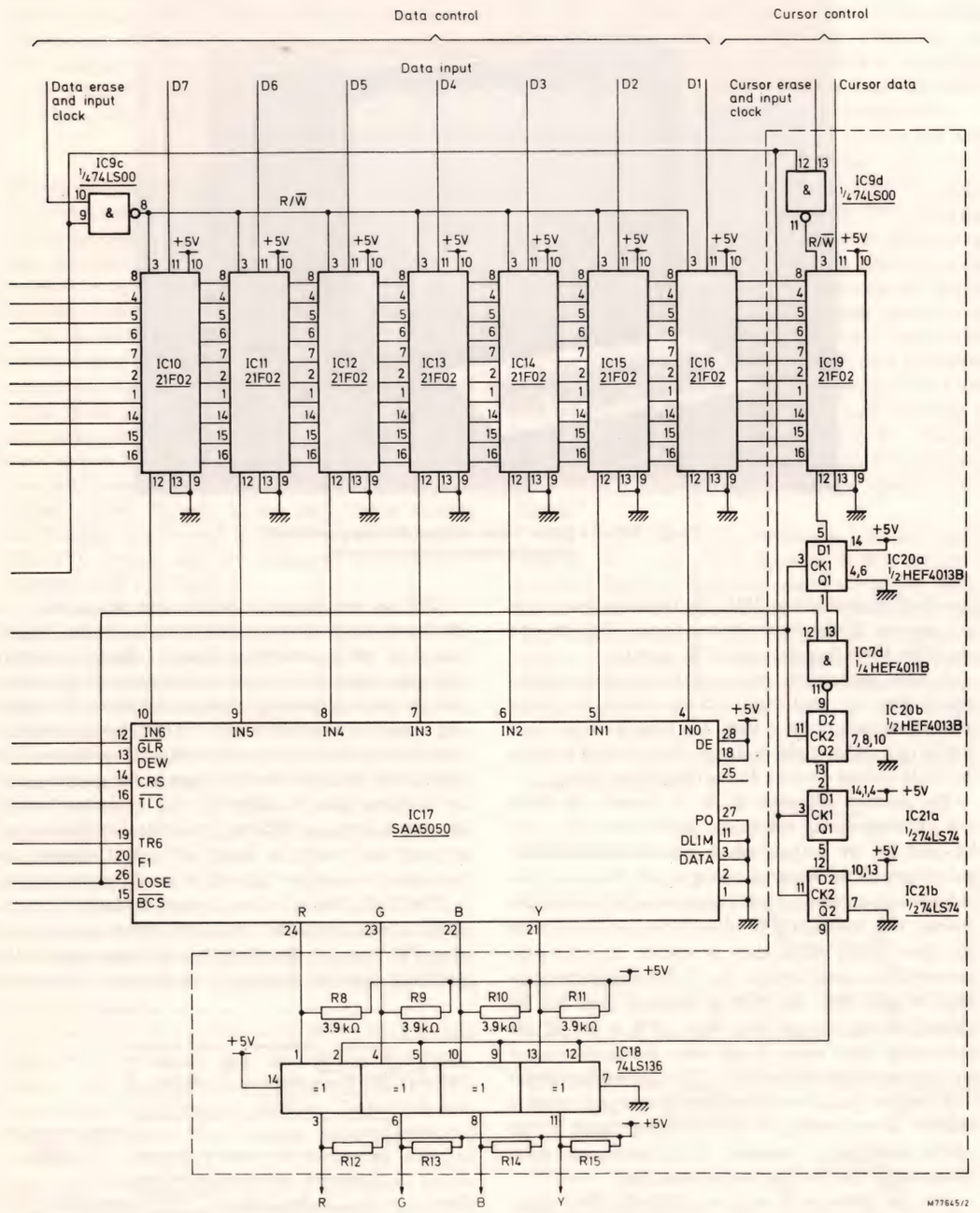


Fig.3 – Part of a typical home terminal showing an adapted television receiver and a keyboard

this clock signal down to 25Hz, the television frame rate, and generate all the display timing signals. Fig.4 shows a simplified block diagram of the TIC circuits.

In this application, most of the functions of the timing chain are used and the chain controls the major timing functions in the system. The Read Address Clock RACK (pin 24) is a 1MHz output which is used to clock the RAM address decoder during the display period.

The memory addresses A_0 to A_4 provide the RAM row addresses during the display period. Pins 3, 4, 7, 11, 13, and 14 are outputs which provide the character generator with the required timing signals. However, two of these outputs also provide signals to other parts of the system. The Data Entry Window DEW (pin 14) defines the time during which data is written into the page memory. This signal is HIGH for 17 lines (approximately 1ms) in each field and thus a complete page can be inserted during a single field scan. DEW is not all the non-display time, but it is used since during this period the memory is directly available. The General Line Reset $\overline{GLR}$ output (pin 7) is a tv line frequency signal which is available as a clocking or synchronising signal to the control equipment, if required. It is a 1μs negative pulse commencing 5μs after the start of each line.

TIC also generates a negative composite sync signal (pin 5). This is an internally-generated signal for use when no incoming tv signal is available. (This output is termed After-Hours Sync $\overline{AHS}$ since, for example, it enables teletext to be displayed outside the hours during which television signals are broadcast.)

TIC has two inputs to enable large characters to be displayed. Large characters are twice the normal height, but their width remains unchanged. Thus the display becomes a page of 12 rows each containing 40 characters, and the store effectively contains two pages. The input Big Character Select $\overline{BCS}$ (pin 17) determines normal or double-height characters, and the input Top/Bottom $\overline{T}/B$ determines which of the two pages in the memory is to be displayed (that is, either the top or bottom half of the page). In this application, the control of these inputs is performed locally as shown in Fig.2. (If desired, the two switches could be replaced by one three-way switch.)

The basic timing of the system is derived from a 6MHz crystal-controlled oscillator, whose output is fed into TIC (pin 2). The effective mark-space ratio of the oscillator must be close to 1:1 in order to obtain satis-

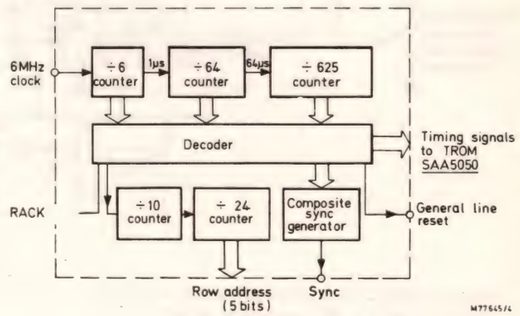


Fig.4 – Timing chain chip TIC (SAA5020)

factory character rounding. Therefore, the oscillator circuit in Fig.2 includes a level-controlled amplifier to keep the centre of the drive waveform at approximately 1.4V, which is the TIC switching threshold.

For detailed information on all the ICs discussed in this article, refer to the published data.

Memory addresser

The display memory addresser has two functions. During the display period of each field it provides the memory read addresses from signals derived from TIC. During the data entry period, the memory addresser passes externally-controlled address instructions to the memory.

The row addresses for the display are provided on five parallel output lines from TIC (pins 19 to 23). The three outputs A_0, A_1, and A_2 (see Fig.2) are only capable of driving MOS loads and thus an HEF4019B LOCMOS multiplexer (IC_6 in Fig.2) is used on these outputs; as these outputs are row addresses, the speed of LOCMOS does not present a problem. The remaining two row-address outputs A_3 and A_4 can carry higher currents and thus they can be used to drive low-power Schottky (LS) TTL devices; they are connected to a 74LS157 multiplexer (IC_5 in Fig.2).

The column addresses for the display are provided by forty pulses from the RACK output of TIC (pin 24). The column addresses have to be handled by low-power Schottky devices because the speed requirements are much more critical than for the row addresses; also the column addresses have to be converted into binary form by a counter. Thus, the pulses from RACK are fed into a binary counter consisting of two 74LS161 devices (IC_2 and IC_3 in Fig.2) and the counter is reset to zero at the beginning of each line by the $\overline{GLR}$ signal from TIC. The six outputs from the binary counter form the 6-bit column addresses and are fed into one of the two 74LS157 multiplexers (IC_4 and IC_5 in Fig.2). The three multiplexers (IC_4, IC_5 and IC_6 in Fig.2) select either the address generated by the timing chain (during the display period), or the externally-generated address (during the data entry period).

As the display is organised as 24 rows of 40 characters (giving 40 columns), the row addresses are 5-bit binary signals, while the column addresses have 6 bits. However, the memories are organised as 32-by-32 matrices with 10-bit address codes. Therefore, the addresses generated by TIC (or externally) must be interfaced with the standard 1k RAMs. This function is performed by the 74LS83A adder (IC_8 in Fig.2) which combines two bits of the row address and three bits of the column address to form four bits of memory address. The four outputs from the adder, together with three outputs from IC_4, and three outputs from IC_6, form the 10-bit address code for the memory.

Display memory

The data for a displayed page of 40-by-24 characters is stored in eight 1024-bit 21F02 static RAMs (IC_{10} to IC_{16}, and IC_{19}, in Fig.2). The memory is partitioned into two sections which have independent Read/Write $R/\overline{W}$ controls, but have a common addressing system.

The principal part of the memory is seven bits wide (IC_{10} to IC_{16}) and is used to store the 7-bit teletext codes for the display and control characters. During the data entry period (defined by DEW), the 'Data Erase and Input Clock' (Fig.2) accepts Write pulses so that text can be written into the memory on the data inputs D_1 to D_7. This input clock is normally LOW during the display period. However, if the displayed page needs to be completely cleared, the data input clock is taken HIGH for one display period, and the SPACE code (0100000) is simultaneously entered into the memory. The 1MHz output F1 from TIC (pin 4) is then used internally to write a space into all the locations in the character memory. Fig.5 shows the timing signals for data entry into the system, while Fig.6 shows the internal timing signals.

The smaller part of the memory is 1-bit wide and is used to store the cursor location if this facility is required. This second memory enables the display system to run completely independently of the control equipment when necessary, since the position of the cursor does not need to be stored externally. The timing of signals to this part of the memory is essentially the same as the timing of the character memory: DEW is gated with the 1MHz signal from TIC and then fed to the cursor $R/\overline{W}$ input during the display period so that the cursor can be erased.

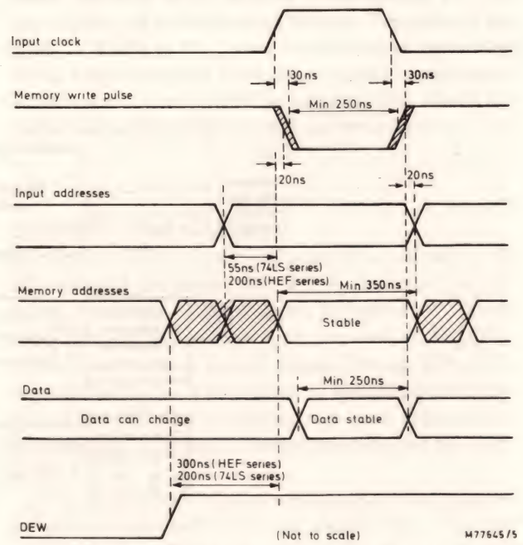


Fig.5 – Timing for data entry into the VDU

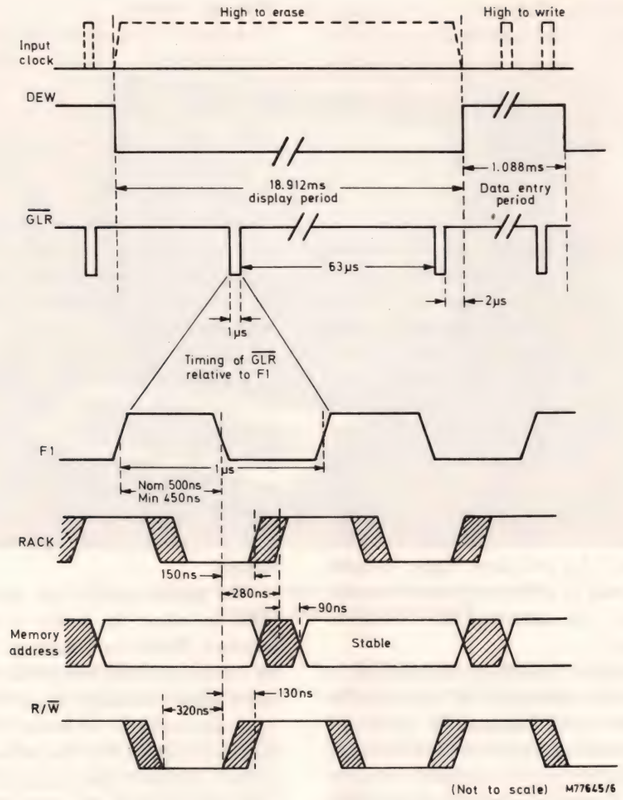


Fig.6 — Internal timing signals (showing timing for page or cursor clear)

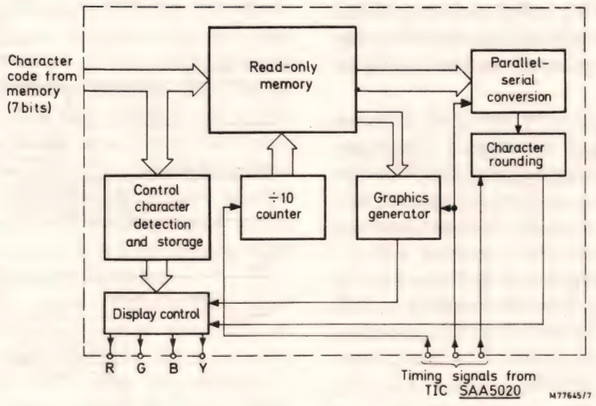


Fig.7 — Character generator chip TROM (SAA5050)

Character generator TROM (SAA5050)

The character generator TROM (IC_{17} in Fig.2) is an MOS n-channel IC which provides the required video drive signals for a teletext display. In response to timing signals from TIC, TROM converts the 7-bit character data from the display memory into a dot matrix pattern. This matrix is in a 7-by-5 dot form for each alphanumeric character, but TROM also contains a character rounding facility which effectively increases this matrix to 14-by-10, thus giving improved definition to displayed characters. The matrix is actually in a 9-by-5 dot form (effectively 18-by-10 with character rounding) since space below the row is provided for those characters with descenders (g, j, p, q, and y); however, no character exceeds 7 dots in height. Character rounding is the process whereby a half dot is inserted before or after a full dot in the presence of a diagonal in a character matrix; it is discussed in detail in Ref.2. Fig.7 shows a simplified block diagram of the TROM circuits.

Additional circuits in TROM enable various control functions to be performed. These functions are determined by control characters (as opposed to alphanumeric and graphics characters) received from the memory. These control characters are discussed in the next section.

The character generator TROM contains no provision for the display of a cursor, and thus additional circuitry is required for this facility (dashed box in Fig.2). The cursor position is stored in a 1024-bit 21F02 RAM (IC_{19} in Fig.2) which has its own R/$\overline{W}$ control; therefore the cursor can be controlled independently of the rest of the equipment. This allows a full display without any input from the control equipment, which is particularly important in a multi-access computer system, for example.

The output from the cursor memory is delayed in a shift register which compensates for the delays to the character data in TROM. The output from the shift register then controls the character generator video outputs (R, G, B, and Y) in a 74LS136 quad exclusive-OR gate (IC_{18} in Fig.2). A '1' in the cursor memory indicates the position of the cursor, and when this '1' is applied to the exclusive-OR gate, the video signals are inverted.

There are two simple methods of controlling the cursor. Firstly, the existing cursor location is addressed during the data entry period and a '0' written into it. A '1' is then written into the new cursor location. The disadvantage of this method is that if the existing cursor is not at the expected address, it would not be erased, and two cursors would appear on the screen. The second method avoids this problem by writing a '0' into every address during the display period, and then writing a '1' into the new cursor position during the following data entry period. However, this second method requires the cursor memory to be separate if the display is to be independent of the control equipment. Therefore, if the eight 1k RAMs in Fig.2 were to be replaced by two 4k RAMs (Signetics types 2614, for example), a separate 1k cursor memory would still be required. This would not be the case with the first method outlined above.

TABLE 1

Teletext Character Codes

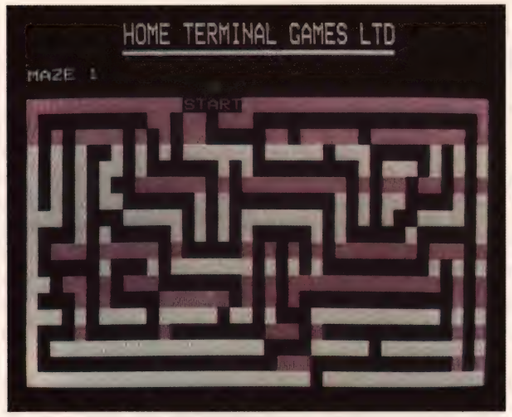
Data bits	b_7	0	0	0	0	1	1	1	1
	b_6	0	0	1	1	0	0	1	1
b_4 b_3 b_2 b_1	b_5	0	1	0	1	0	1	0	1
0 0 0 0		NUL*	DLE*	▯	▯	0	P	—	p
0 0 0 1		Alpha^n Red	Graphics Red	!	1	A	Q	a	q
0 0 1 0		Alpha^n Green	Graphics Green	"	2	B	R	b	r
0 0 1 1		Alpha^n Yellow	Graphics Yellow	£	3	C	S	c	s
0 1 0 0		Alpha^n Blue	Graphics Blue	$	4	D	T	d	t
0 1 0 1		Alpha^n Magenta	Graphics Magenta	%	5	E	U	e	u
0 1 1 0		Alpha^n Cyan	Graphics Cyan	&	6	F	V	f	v
0 1 1 1		Alpha^n White	Graphics White	'	7	G	W	g	w
1 0 0 0		Flash	Conceal Display	(	8	H	X	h	x
1 0 0 1		Steady	Contiguous Graphics	)	9	I	Y	i	y
1 0 1 0		End Box	Separated Graphics	*	:	J	Z	j	z
1 0 1 1		Start Box	ESC*	+	;	K	←	k	¼
1 1 0 0		Normal Height	Black Background	,	<	L	½	l	‖
1 1 0 1		Double Height	New Background	−	=	M	→	m	¾
1 1 1 0		SO*	Hold Graphics	.	>	N	↑	n	÷
1 1 1 1		SI*	Release Graphics	/	?	O	#	o	■

Black represents display colour, and white represents background.
*These control characters are reserved for compatibility with other data codes.

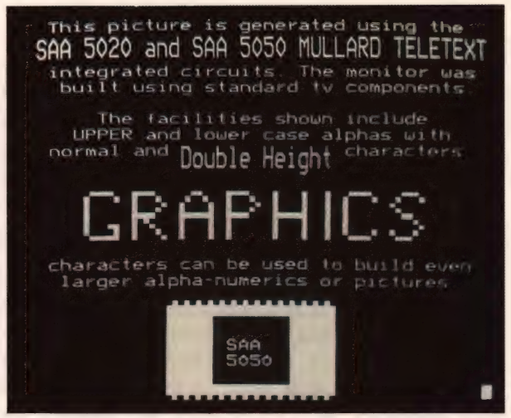
CONTROL CHARACTERS

The teletext 7-bit data code provides a full set of 96 alphanumeric characters, 64 graphics characters, and 32 control characters. Table 1 shows the full set of teletext codes. The control characters are decoded by TROM to produce the required display format, but are themselves displayed as blanks. A description of the effects produced by the teletext control characters is given below. Fig.8 shows several examples of screen displays from the VDU in Fig.3.

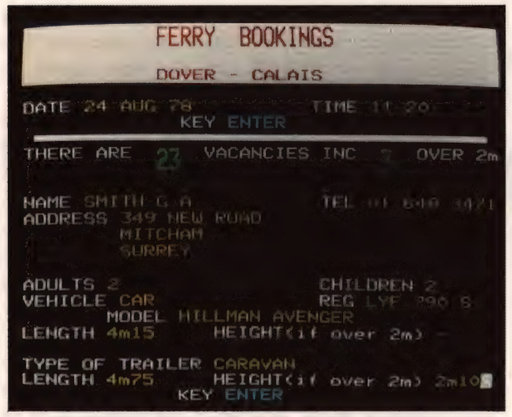
Note that some of the control characters are reserved for compatibility with other data codes, while others are unsuitable for VDU applications. Also, seven of the codes are known as 'default codes': they apply to a



(a)

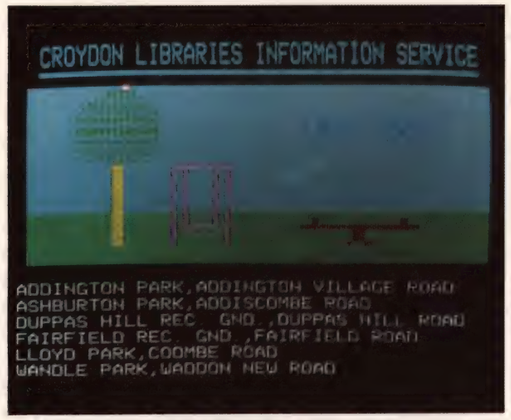

This picture is generated using the
SAA 5020 and SAA 5050 MULLARD TELETEXT
integrated circuits. The monitor was
built using standard tv components
The facilities shown include
UPPER and lower case alphas with
normal and Double Height characters
GRAPHICS
characters can be used to build even
larger alpha-numerics or pictures
SAA
5050

(d)



(b)

(e)


CROYDON LIBRARIES INFORMATION SERVICE
ADDINGTON PARK,ADDINGTON VILLAGE ROAD
ASHBURTON PARK,ADDISCOMBE ROAD
DUPPAS HILL REC GND.,DUPPAS HILL ROAD
FAIRFIELD REC GND.,FAIRFIELD ROAD
LLOYD PARK,COOMBE ROAD
WANDLE PARK,WADDON NEW ROAD

(c)

Fig.8 – Various examples of screen displays generated using the logic circuit described in this article
(a) Video game
(b) Possible form of a display in a travel agency. (The cursor can be seen in the bottom right-hand corner.)
(c) Possible information display showing how coloured graphics might be used. The example shown is for illustration only
(d) Monochrome display showing several of the available facilities
(e) Possible information display showing both contiguous and separated graphics, and double-height characters

'normal' display and are assumed before each row begins. These controls are: 'alphanumeric white', 'black background', 'contiguous graphics', 'normal height', 'non-flashing', 'release graphics', and 'end box'.

Coloured characters

The alphanumeric characters can be displayed on the screen in any of seven colours, depending on the alphanumeric control character chosen. These colours are: red, green, yellow, blue, magenta, cyan, and white.

Graphics characters

Each of the 64 graphics characters can be in any of the seven standard colours above. The use of these characters permits the construction of extra large letters and simple diagrams (such as weather maps). Graphics characters are displayed on a 2-by-3 matrix as shown in Fig.9. Six bits determine which cells on the matrix are illuminated, while the seventh bit (b_6) distinguishes between alphanumeric and graphics characters. If b_6 is a '0', then the code is always for an alphanumeric character, if it is a '1', then the code is either for an alphanumeric or a graphics character; the control characters determine which.

The control characters 'contiguous graphics' and 'separated graphics' allow different areas of graphics or outlines to be distinguished by either being contiguous (a continuous line, for instance) or being separated (a dotted line, for instance), see Fig.10.

The 'hold graphics' control character enables the blanks on the display produced by the control characters to be filled by a repeat of the preceding graphics character. Thus, for example, different coloured areas in graphics can be joined up without gaps between them. The command 'release graphics' cancels this control.

Coloured backgrounds

The background of a display is normally black, but a background of any of the seven standard colours can be selected by the control character 'new background'. The background then becomes the colour of the preceding alphanumeric colour control character. A black background is restored by the control character 'black background'.

Flashing characters

All characters following the control 'flash' flash repetitively until the command 'steady' is received.

Double-height characters

The control 'double height' causes the characters following it to be displayed twice the normal height but with the same width, and thus selected characters can be displayed double-height. The command 'normal height' cancels this command.

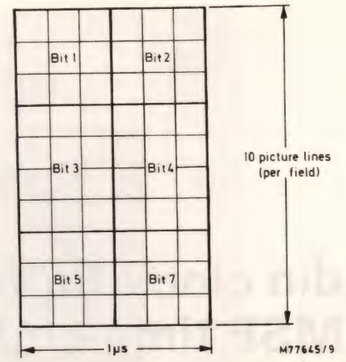


Fig.9 – Allocation of data bits to a graphics character and the size of the character rectangle

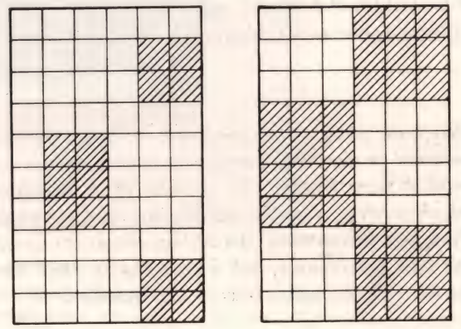


Fig.10 – Graphics character 1100110
(a) separate mode (b) contiguous mode

Box and conceal

The 'start box' and 'end box' control characters allow the normal video signal to be blanked out in chosen areas and thus, for instance, a box can be generated around a subtitle or newsflash. However, it seems unlikely that this facility has any application in VDUs.

The control character 'conceal display' causes part of the display to be suppressed and stored in the memory until required. Thus, in teletext applications, the broadcasters can conceal an answer to a question. Normally, suppressed characters are designed to be revealed by a remote control/receiver system, but they can be revealed by blanking out the control character 'conceal display' and so this facility may be useful for VDUs.

REFERENCES

1. 'Teletext – the LSI solution', Technical Information 54, TP1606, Mullard Limited, 1977.
2. KINGHORN, J.R., 'Character rounding for alphanumeric video display', **Mullard Technical Communications**, Vol.13, No.126, April 1975, pp.230 to 239.

Radio clock for reception and display of MSF time-code transmission

P.G. GILES, P.J. HART, and I. THOMAS
Mullard Application Laboratory

Details are given of the coded time and date information included in the MSF standard frequency 60kHz transmission from Rugby, UK. A radio clock is described which receives, decodes, and displays time information from this transmission. An add-on circuit for decoding the date information, and a slave-display clock circuit for use with the radio clock, are also described.

INTRODUCTION

The National Physical Laboratory (N.P.L.) includes coded time and date information on the 60kHz MSF standard frequency transmission from Rugby, UK. ('MSF' is the call-sign allocated to this transmission.) Since 1974, the service has carried binary-coded time-of-day information, updated each minute. In November 1976, binary-coded calendar information, and an additional data bit to indicate when Greenwich Mean Time (GMT) and British Summer Time (BST) are in operation, were added to the transmission. The area served by the transmission covers the United Kingdom and Western Europe, including Iceland and Finland.

A radio clock which is suitable for the reception and display of this information has been developed by Mullard, and is described, together with constructional details, in this article. The laboratory prototype radio clock is shown in Fig.1. This clock provides a display of hours, minutes, and seconds, but an add-on circuit to provide a display of the date is also described in Appendix 1. It is possible to use the clock as a master to drive a number of remote slave-display clocks such as that described in Appendix 2.

Before the radio clock is considered, a description is given of the three types of data inserted into the 60kHz MSF transmission.

TRANSMITTED SIGNAL

Apart from its function as a frequency standard, the Rugby MSF 60kHz transmission includes coded time and date information transmitted in the form of a 'fast code' and two separate 'slow codes'. (It is the fast code that is used by the Mullard radio clock.)

Fast-code transmission

The fast-code transmission is termed 'fast' because, unlike the two slow codes, it occupies only the first 330ms of each minute. This transmission gives the time, day, and month, coded as shown in Fig.2.

The transmission starts with two pulses: a 20ms control pulse transmitted 25ms after the minute edge, and a 10ms marker pulse transmitted 5ms after the control pulse. All the remaining pulses in the transmission have a pulse-width of 10ms. The time code is transmitted next, consisting of 13 bits of binary-coded decimal (BCD) information followed by a parity bit. The time code provides hours and minutes in the Coordinated Universal Time (UTC) scale which, in practical terms, is equivalent to Greenwich Mean Time. After the parity bit, a 'BST ON' bit is transmitted during British Summer Time. This bit can be used to add automatically one hour to the time displayed by the decoder. (This facility is incorporated in the Mullard circuit.) After the 'BST ON' bit, a further 11 bits are transmitted, giving the day and month code, followed by a final parity bit.

The addition of an extra hour to the display during

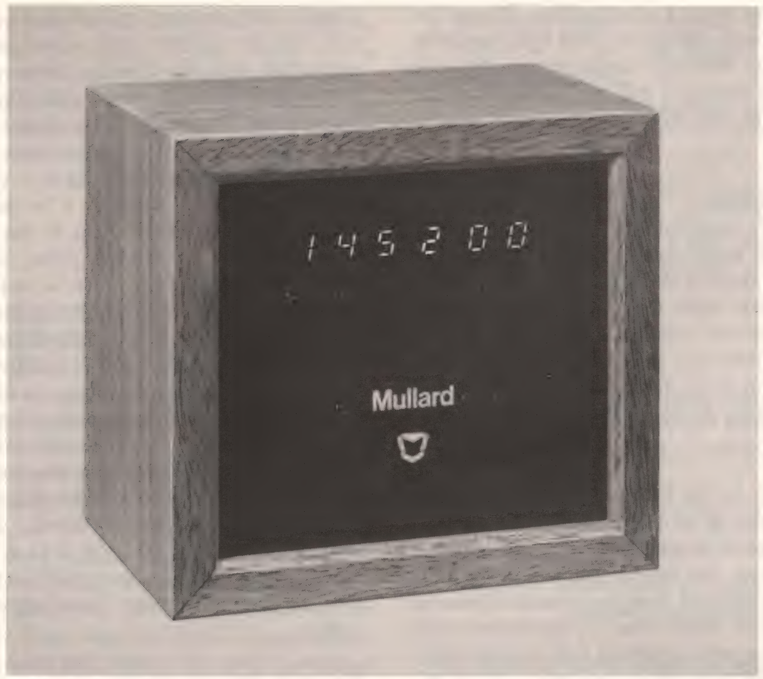


Fig.1 — Laboratory prototype radio clock.
It is not proposed by Mullard Limited to manufacture or market such a clock in an assembled form

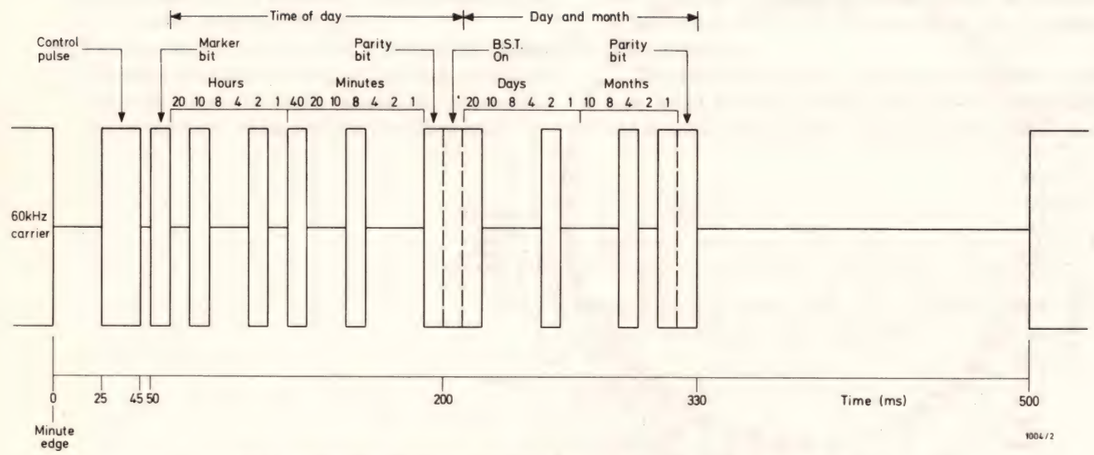


Fig.2 — Fast-code information inserted in Rugby MSF standard frequency 60kHz transmission. The time indicated in bit-form is 12.48 BST, 22nd May

BST does, however, create a minor problem. Because the transmitted date code changes at 2400 GMT regardless of the time of year, MSF radio clocks using the fast-code transmission, and displaying BST will show a change in date one hour *after* 2400 BST.

Slow-code transmission

The two slow-code transmissions are completely independent of each other and of the fast-code transmission, and each has its own form of bit-coding. The first is termed 'DUT1' (the letters stand for 'Difference of Universal Time'), and the second transmission provides time, day, and month information as given by the fast-code transmission, but also includes the last two digits of the year and a digit to identify the day of the week.

DUT1

Time information to the UTC scale as transmitted by MSF is derived from an 'atomic clock'; that is, one using a caesium standard. It is from such a clock that Atomic Time AT is derived. The seconds markers of the UTC scale and the atomic time scale are identical in interval and epoch. However, atomic time and time derived from the rotation of the earth (Universal Time 1, or UT1) are not necessarily the same throughout the year. At the beginning of the year, UT1 might lag UTC by a fraction of a second and, by the end of the year, might lead it by a similar amount. For this reason, the UTC scale is adjusted when necessary in steps of one complete second such that the two time scales remain within ±700ms of each other. It is this difference between UT1 and UTC that is provided, to an accuracy of ±50ms, by the DUT1 transmission. The DUT1 coded information is transmitted during the period extending from the first to the sixteenth second, as shown in Fig.3.

Each second is marked by a 'normal', or uncoded, carrier drop-out pulse of 100ms. In the DUT1 transmission, the number of seconds pulses, coded as double pulses between one and seven seconds, indicates the number of 100ms steps that UT1 is *ahead* of UTC. For example, coded pulses transmitted for the first two seconds would indicate that UT1 is 200ms *ahead* of UTC (UT1 – UTC = +200ms). The number of seconds coded between eight and fifteen seconds indicates the number of 100ms steps that UT1 is *behind* UTC. For example, coded pulses transmitted for the ninth, tenth, and eleventh seconds would indicate that UT1 is 300ms *behind* UTC (UT1 – UTC = –300ms).

If, at the end of the year, UT1 is more than one second ahead of UTC, a 'leap second' is included for the following year to indicate the adjustment in the UTC scale.

Slow-code time-and-date information

The slow-code time-and-date information is transmitted over the period between the 17th and 59th seconds, as shown in Fig.3. The carrier drop-out pulses, occurring each second, are coded for this transmission by extending their width from the normal 100ms (binary '0') to 200ms (binary '1'). Normal BCD coding is used for the transmitted information, consisting of the year, month, day-of-month, day-of-week, hour, and minute. A group of 'minute identifier' pulses are then transmitted, including the parity bits for the slow-code time-and-date information.

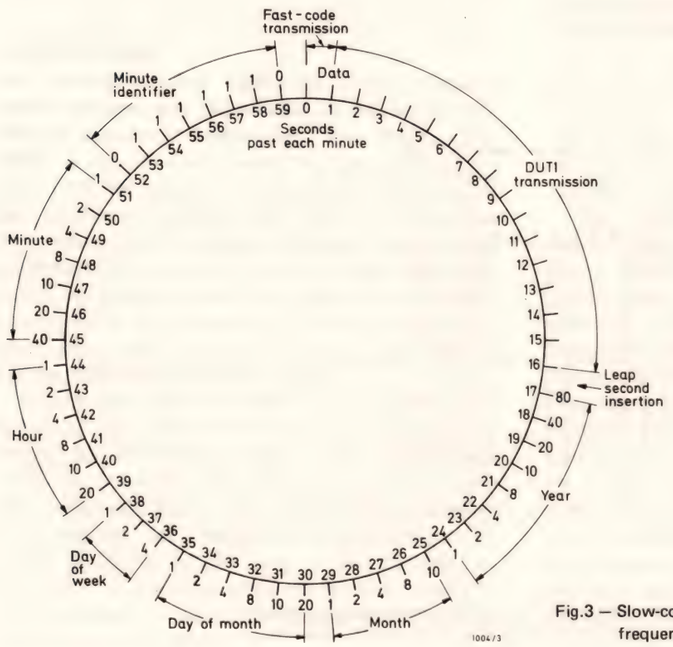


Fig.3 – Slow-code transmissions inserted in Rugby MSF standard frequency 60kHz transmission

PRINCIPAL FEATURES OF MULLARD RADIO CLOCK

The Mullard radio clock receives, decodes, and displays time information derived from the MSF fast-code transmission described earlier. The principal features of this clock are outlined below.

- Within the first minute of being switched on, the clock is automatically set by the transmission to the correct time, and will be reset in the same way following power failure or signal failure. The period required after switch-on before the clock displays the time depends on the actual moment of switch-on; the longest time being when the clock is energised just after the minute information has been transmitted. The clock will then take up to 59s before it receives the next minute BCD information and displays it. (The minimum waiting time is about one second if the clock is energised just before the minute signal.)
- In response to the 'BST ON' bit, when this is transmitted, the clock will automatically display British Summer Time during the summer months. In the absence of the bit (during the winter months), the clock reverts to a display of GMT.
- The clock provides a digital display of hours, minutes, and seconds, and an additional circuit described later can be added to display the date.
- The decoder and GMT-to-BST converter use Mullard LOCMOS integrated circuits, and are thus suitable for large-scale or medium-scale integration, or construction on a printed-wiring board as described later.
- The 60kHz receiver is pretuned, and uses the Mullard TDA1050 r.f., i.f., and detector integrated circuit, which includes a.g.c.
- The clock can be used as a self-contained unit, or as a master clock to drive a number of remote slave-display clocks. The use of slave-display clocks results in a saving in component cost because of the simplified circuit compared with that of the complete MSF radio clock. Details of a slave-display clock and the interface circuits are given later.

OPERATION

A block diagram of the Mullard radio clock is shown in Fig.4. The laboratory prototype clock is constructed on three printed-wiring boards, containing the circuits listed below:

board 1	receiver and power supply;
board 2	decoder and GMT-to-BST converter;
board 3	multiplexing and driver circuits, and six 7-segment numerical displays.

Full details of these boards are given later, while the circuits on each board are described below. On the circuit diagrams shown in Figs.6 to 9, 20, and 22, the circled letters indicate interconnection points between circuits. The remaining letters indicate connection points on the printed-wiring boards.

Receiver

The circuit of the receiver is shown in Fig.5, and uses the TDA1050 integrated circuit. This IC is primarily intended for use in a.m. car radio superhet receivers, but operates in this circuit as a tuned-radio-frequency (t.r.f.) receiver with built-in a.g.c.

The bandwidth of the receiver is determined by the four tuned circuits (including the ferrite-rod aerial L_1), and is about 1kHz at the –3dB points. The output from

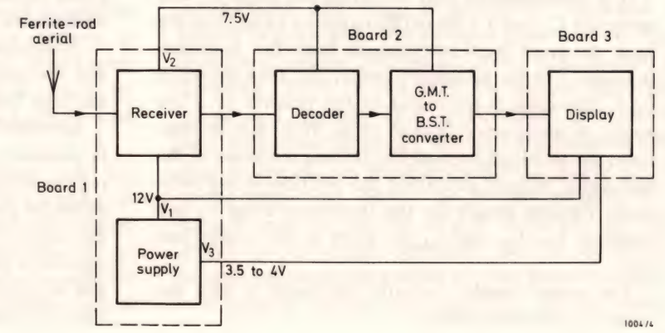


Fig.4 – Block diagram of Mullard radio clock

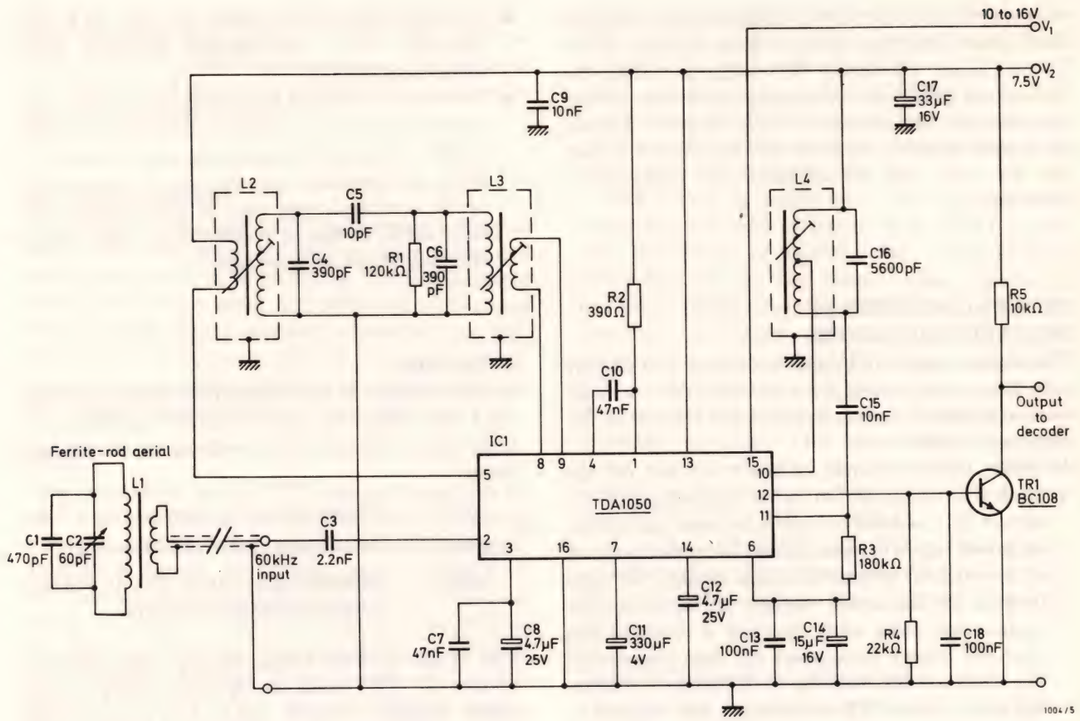


Fig.5 – 60kHz receiver

IC_1 is d.c.-coupled to TR_1, which provides an output signal of about 7V to the decoder for an input signal of 2μV from the aerial. The a.g.c. time-constant is set by C_{11}, and is large enough to prevent the gain of the receiver changing substantially during periods of zero carrier in the transmission.

The TDA1050 includes a voltage stabiliser which gives a nominal output voltage for the receiver of 7.5V from an unstabilised input of 10 to 16V. The output from this stabiliser is also used to supply the decoder and GMT-to-BST converter circuits.

It is recommended that the ferrite-rod aerial L_1 and capacitors C_1 and C_2 should be mounted away from the clock to avoid local interference from the multiplex oscillator. For the laboratory prototype clock shown in Fig.1, the aerial is connected to the receiver by a 2m length of audio-grade coaxial cable. With this arrangement, the aerial can be sited for the best reception of the MSF signal without disturbing the position of the radio clock. Winding details for the ferrite-rod aerial L_1 and inductors L_2, L_3, and L_4 are given in the component lists.

The power supply, mounted on board 1 with the receiver, is described later.

Decoder

A block diagram of the decoder is shown in Fig.6, and the circuit of the decoder is shown in Fig.7.

All the timing pulses for the decoder are derived from a crystal oscillator operating at 3.2768MHz. The output signal from this oscillator is divided by 2^{14} by IC_2, to give 5ms pulses. These pulses are synchronised with the incoming MSF signal, and are then further divided and counted to generate clock pulses for the BCD time data. The clock pulses are also used for the generation of seconds information. Resynchronisation of the 5ms pulses occurs every 60 seconds, immediately before the transmission of the fast-code data.

Integrated circuits IC_{1B} and IC_{1C} form the oscillator, and the divider chain comprises IC_2, IC_3, IC_{1A}, IC_{5A}, and IC_6. The seconds are synchronised by IC_{5B}.

Integrated circuits IC_{16} and IC_{17} form a 16-bit serial-in parallel-out shift register. Clock pulses for this shift register are provided at 10ms intervals by IC_8, and these pulses are gated to start at 55ms, and end at 205ms, after the minute edge. The gating and clocking of the shift register is provided by IC_8, IC_{10A}, IC_{13}, IC_{14}, IC_{15A}, and IC_{11B} to IC_{11F}. The BCD time data is clocked in to the shift register and is converted to parallel form at the

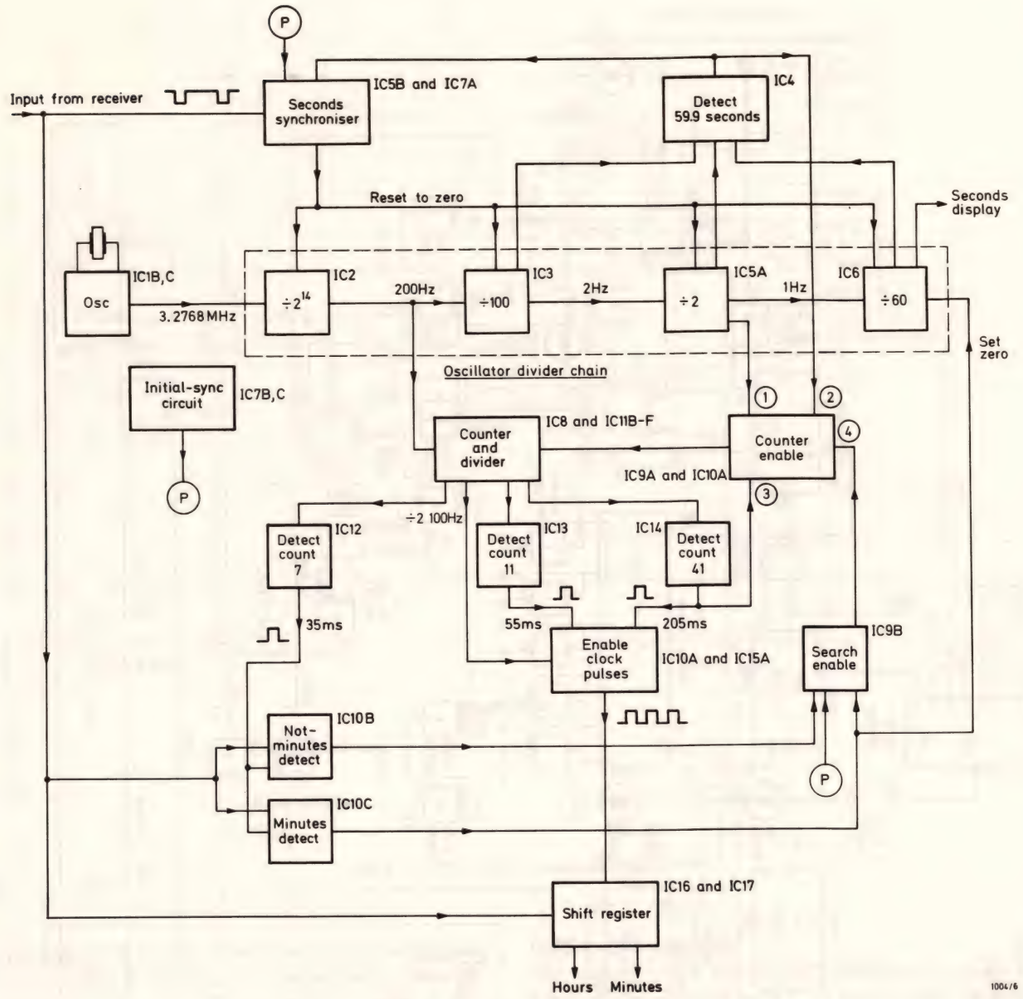


Fig.6 – Block diagram of decoder

outputs of IC_{16} and IC_{17} for display during the minute.

When the seconds divider-and-counter integrated circuits IC_{3B}, IC_{5A}, and IC_6 have reached a count of 59.9 seconds, the main divider chain is reset to zero by IC_4, and the seconds synchroniser is set in readiness to be synchronised with the incoming signal. At the same time, the counter-enable integrated circuit IC_{9A} is set by the signal at point 2 to enable IC_8 to clock minute data in to the shift register.

Integrated circuit IC_{9A} is reset, 205ms after the minute edge, by the signal at point 3, and IC_8 is switched off. This resetting of IC_{9A} occurs once every 60 seconds, provided that the minute detector (comprising IC_{10B}, IC_{10C}, and IC_{12}) has detected the incoming minute data. The minute detector responds to the 20ms control pulse, the centre of which occurs 35ms after the minute edge (see Fig.3). If no pulse is detected, a 'not-minute' pulse is generated, and the output (point 4) of the search-enable latch IC_{9B} is set HIGH. The signal at point 4 is gated with 1Hz pulses at point 1, to set IC_{9A} once every second. Integrated circuit IC_{9A} is reset as described earlier, 205ms after the minute edge. This setting and resetting of IC_{9A} continues until minute data is detected by IC_{10C}, and the search-enable latch IC_{9B} is cleared. The seconds-counter IC_6 is reset to zero at the same time. Hence, the decoder searches every second until the minute data is detected, and then reverts to its normal operation; that is, to wait 60 seconds before clocking-in the data for the next minute.

Integrated circuits IC_{7B} and IC_{7C} set the seconds

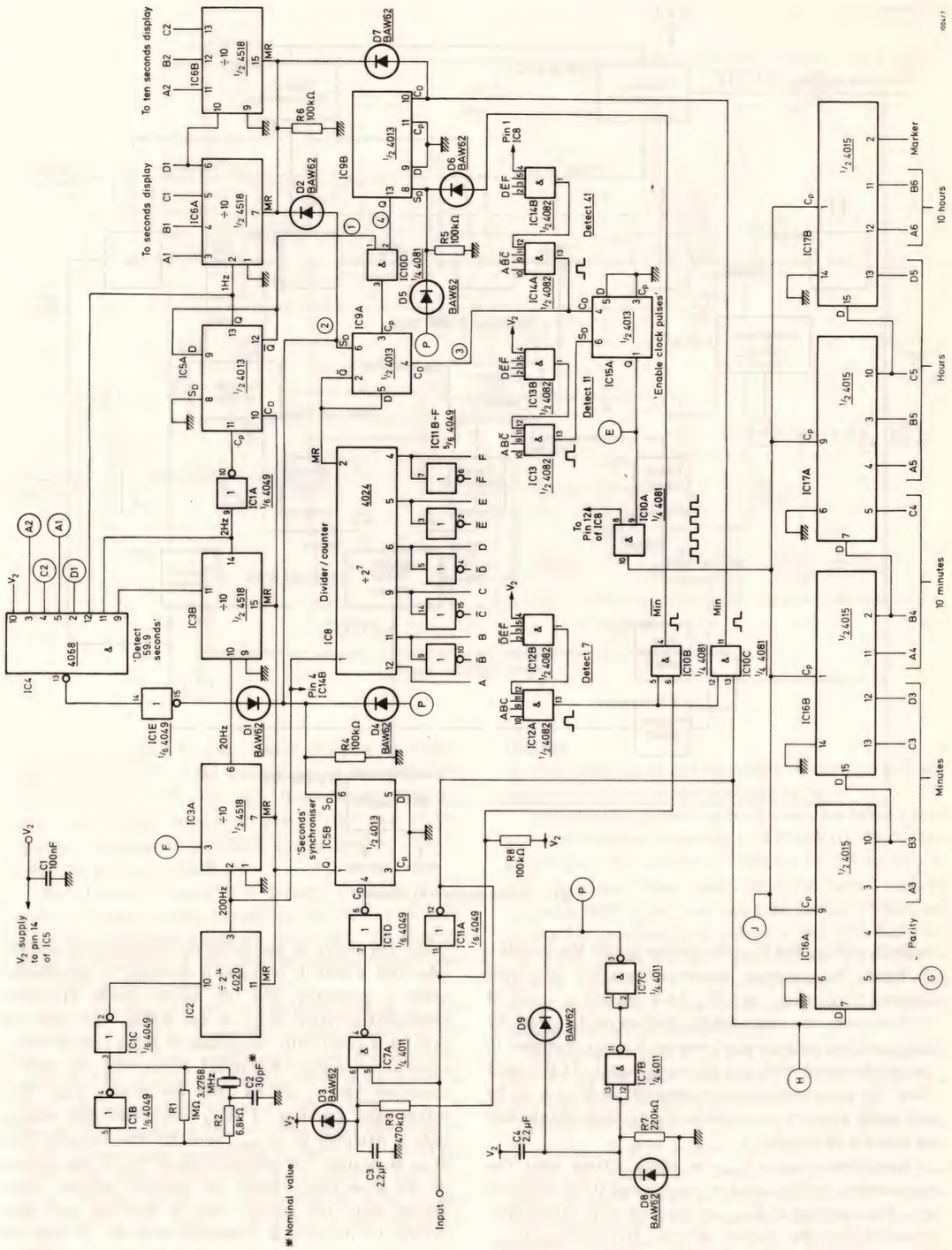
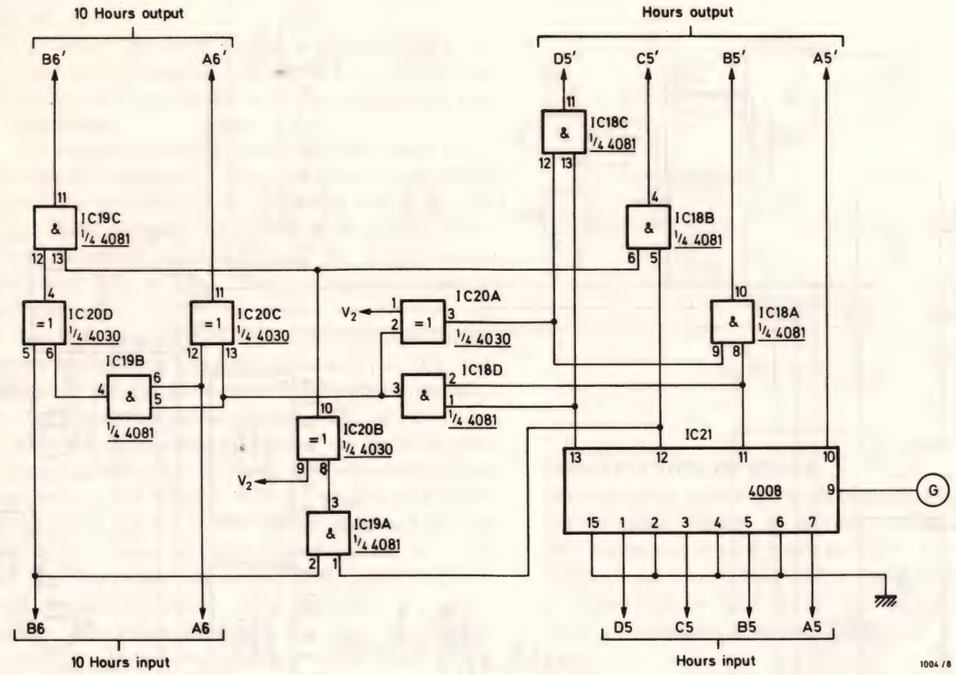


Fig.7 — Decoder

Supply pins

Integrated circuit	Pin V_{SS}	Pin V_{DD}
IC_1, IC_{11}	8	1
IC_2, IC_3, IC_6, IC_{16}, IC_{17}	8	16
IC_4, IC_5, IC_7 to IC_{10}, IC_{12} to IC_{15}	7	14



Supply pins

Integrated circuit	Pin V_{SS}	Pin V_{DD}
IC_{18} to IC_{20}	7	14
IC_{21}	8	16

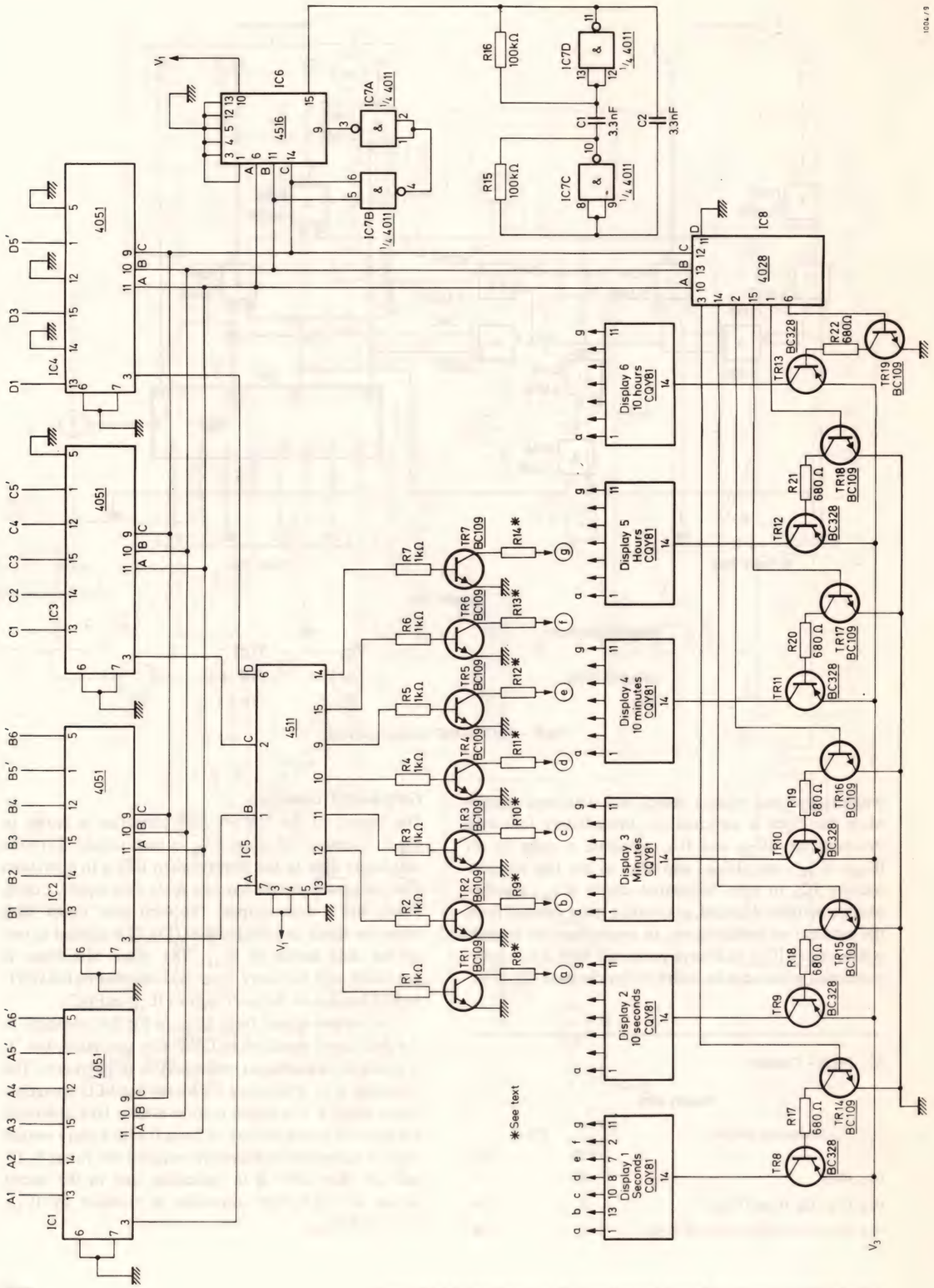
Fig.8 — GMT-to-BST converter circuit

synchroniser and minute search and detection circuits when the clock is switched on. Immediately following switching on, IC_{7B} and IC_{7C} generate a pulse to set IC_{5B}, IC_{9A}, and IC_{9B}, and also to set the seconds-counter IC_6 to zero. Integrated circuit IC_{7A}, together with its peripheral circuit, generates a pulse delayed from the moment of switching on, to ensure that the seconds synchroniser IC_{5B} is always presented with a correctly-positioned pulse-edge on which to synchronise.

GMT-to-BST converter

The circuit of the GMT-to-BST converter is shown in Fig.8. A binary full-adder IC_{21} is used to add '1' to the unit-hours digit in the display when BST is in operation. This integrated circuit has two 4-bit data inputs, a carry input, and a 4-bit output. The 4-bit unit 'hours' data from the signal decoding circuit (Fig.7) is applied to one of the data inputs of IC_{21}. The other data input is grounded, and the carry input is connected to the GMT-to-BST bit-slot of the shift register IC_{16} in Fig.7.

The output signal from IC_{21} in Fig.8 is identical to the data input signal when GMT is in operation, but '1' is added to this output when BST is in operation. The full-adder IC_{21} is intended for binary not BCD operation. Hence when a '1' is added to hour 9, hour 10 is generated for the unit hours instead of hour 0 with a carry output of 1. A correction is therefore required for hours 9, 19, and 23 when BST is in operation, and in the circuit shown in Fig.8, this correction is provided by IC_{18}, IC_{19}, and IC_{20}.



Display

The circuit of the display section is shown in Fig.9. Six common-anode 7-segment LED displays type CQY81 are used, mounted on board 3 with the multiplexing and driving circuits.

The multiplex oscillator, consisting of IC_{7C} and IC_{7D}, operates at a frequency of 2kHz. The multiplex addresses 0 to 5 are generated by IC_6, together with IC_{7A} and IC_{7B}. These addresses are applied to IC_8 and used to select each digit in turn through the driver circuit. Transistors TR_8 to TR_{13} drive the common anode of each display.

The BCD data for each digit is selected sequentially by the multiplexing integrated circuits IC_1 to IC_4, and decoded by the 7-segment decoder integrated circuit IC_5, to drive the segment-driver transistors TR_1 to TR_7.

Resistors R_8 to R_{14} determine the peak current flowing through each segment, and thus control the brightness of the displays. With V_3 equal to 3.5 to 4V (as provided by the power supply described in this article), the value of each resistor should be 6.8Ω (CR25). This supply voltage has been chosen for minimum thermal dissipation within the clock. For other voltages, the values of R_8 to R_{14} must be changed accordingly. Typical examples are: 100Ω (PR37) for a 12V supply, or 56Ω (CR37) for a 7.5V supply.

Power supply

Three supplies are required for the clock, two of which (V_1 and V_3) are provided directly by the circuit shown in Fig.10. The third supply, V_2, is derived from the receiver integrated circuit shown in Fig.5, which includes a voltage stabiliser. The low current drain of the Mullard LOCMOS ICs used in the decoder will not exceed the rating of the internal stabiliser circuit of the TDA1050.

No smoothing capacitor is used for supply V_3 because the LED displays operate satisfactorily from an unsmoothed full-wave rectified supply. The value of 3.5 to 4V for V_3 enables each display to have equal brightness without excessive thermal dissipation from the driver circuits.

◁ Fig.9 — Display circuit

Supply pins

Integrated circuit	Pin V_{SS}	Pin V_{DD}
IC_1 to IC_6, IC_8	8	16
IC_7	7	14

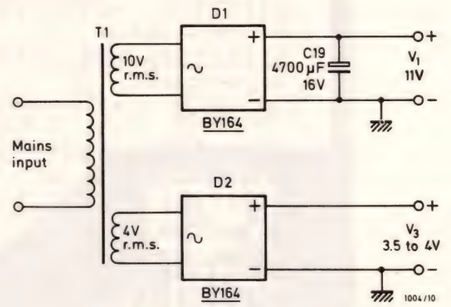


Fig.10 — Power supply

CONSTRUCTION OF CLOCK

The laboratory prototype clock is constructed on three printed-wiring boards, as shown in Figs.11 to 18. The dimensions of each board are 127 X 111 X 1.6mm. Boards 1 and 3 are copper-clad on one side, and board 2 is copper-clad on both sides. The boards should be mounted vertically, separated by spacers, as shown in Fig.19.

All the leads to components on the receiver and power supply board 1 (Figs.11 and 12) should be kept as short as possible, and the clips securing the cups of the pot-cores should be grounded to the board.

For the signal decoder and GMT-to-BST converter board (Figs.13 to 16), either through-hole-plating or wire links can be used to connect the points indicated in Fig.14. Where wire links are used, these should be inserted and soldered on both sides before the components are mounted. The following components require soldering to both sides of the board: IC_5 and IC_6; R_3, R_5, and R_6; and C_1 and C_4. Provision is made on the board for two capacitors to be used for C_2, thus simplifying the adjustment of the crystal oscillator frequency.

Fifteen wire links are required for the display board (Figs.17 and 18), and these should be inserted and soldered before the components are mounted. Interconnections between the boards should be made with fine-gauge insulated multi-strand wire.

Details of the supply pins of the integrated circuits shown in Figs.7, 8, 9, 20, and 22 are given in the tables inset in these diagrams. Some of the sections of IC_1, IC_7, and IC_{15} in Fig.7, and IC_{19} in Fig.8, are not used. For this reason, pin 11 of IC_1, pin 9 of IC_7, pins 8 to 11 of IC_{15}, and pins 8 and 9 of IC_{19} are connected to ground on the printed-wiring boards shown in Figs.11 to 19. If these boards are not used in the construction of the radio clock, then care should be taken to ensure that these pins are still connected to ground.

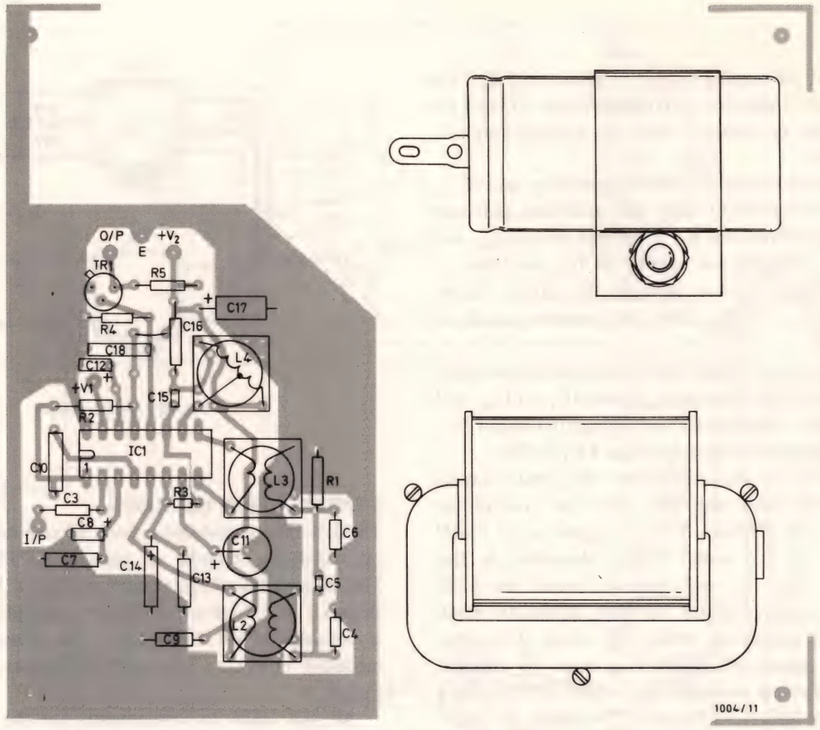


Fig.11 — Component layout of printed-wiring board 1, comprising 60kHz receiver and power supply (actual size)

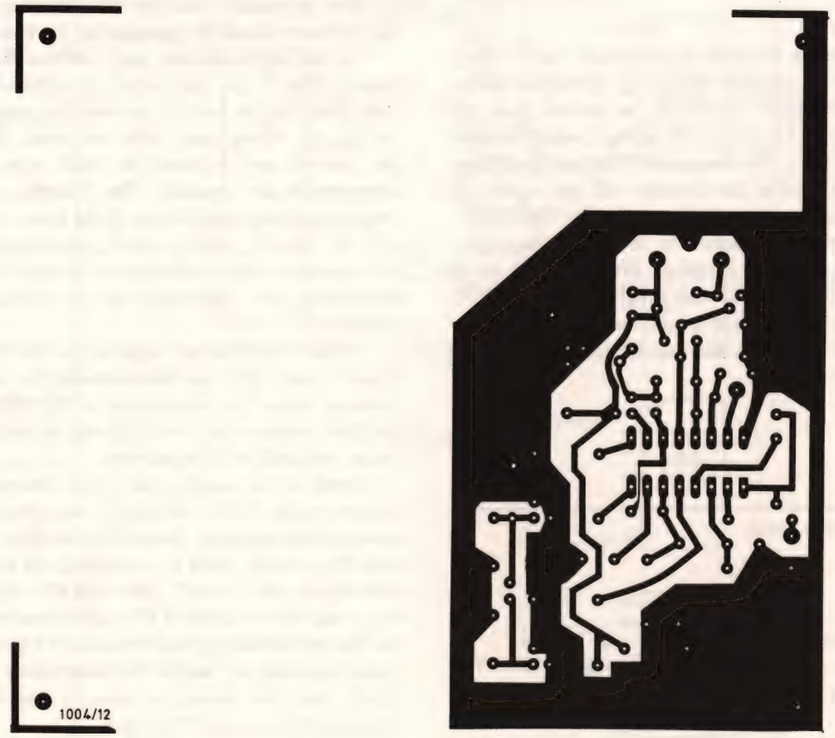
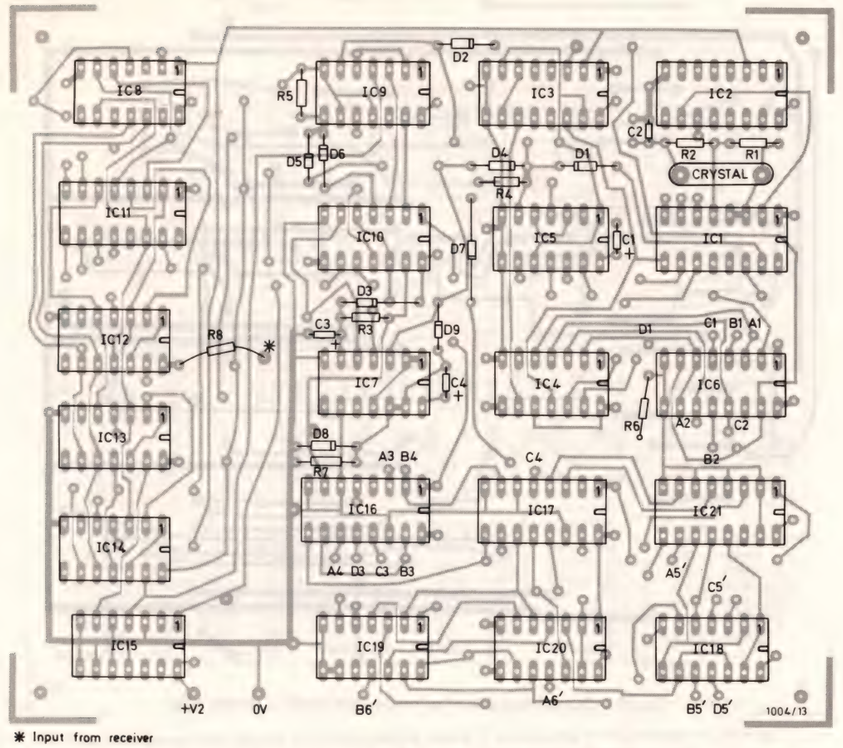


Fig.12 — Copper side of printed-wiring board 1 (actual size)



* Input from receiver

Fig.13 — Component layout of printed-wiring board 2, comprising decoder and GMT-to-BST converter. (Printed track is shown for reverse side of board only, actual size)

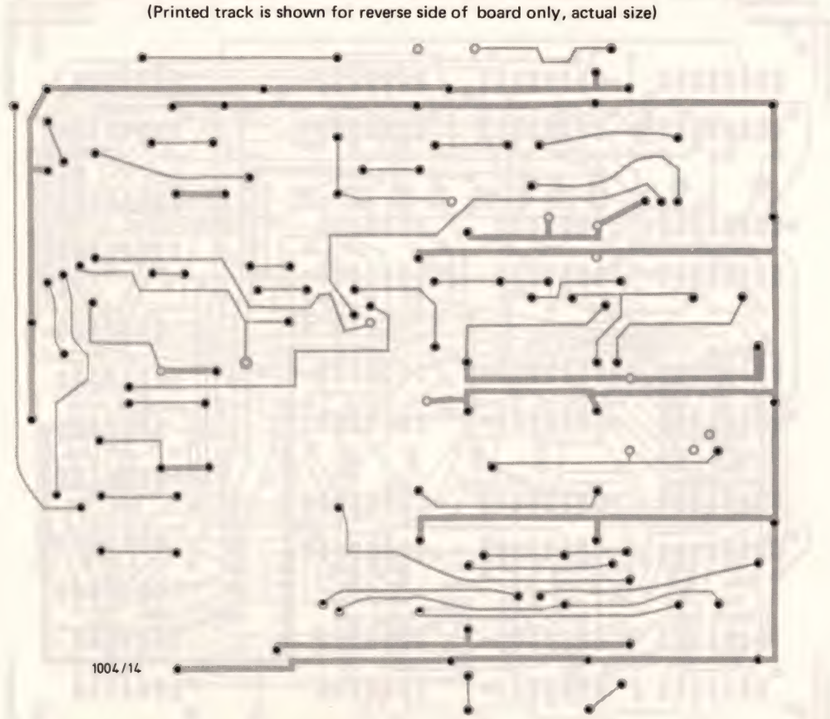


Fig.14 — Points on component side of board 2 (indicated by dots) requiring connection through to corresponding points on reverse side (actual size)

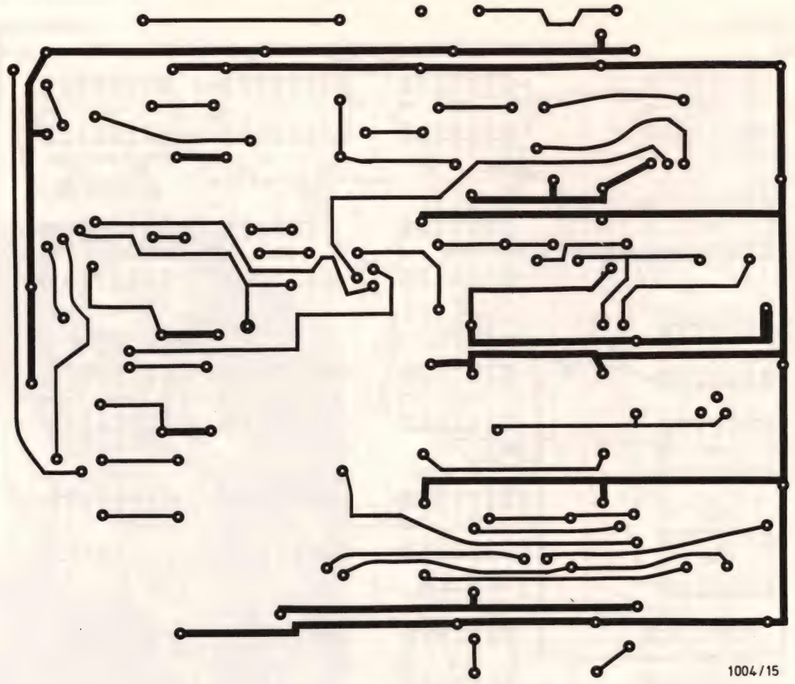


Fig.15 — Component side of printed-wiring board 2 (actual size)

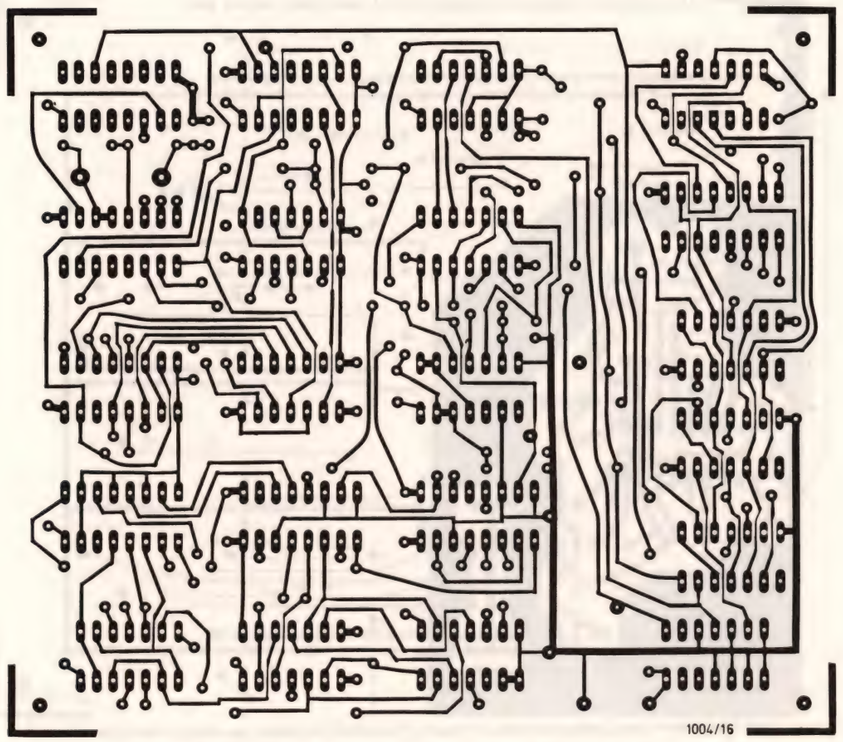


Fig.16 — Reverse side of printed-wiring board 2 (actual size)

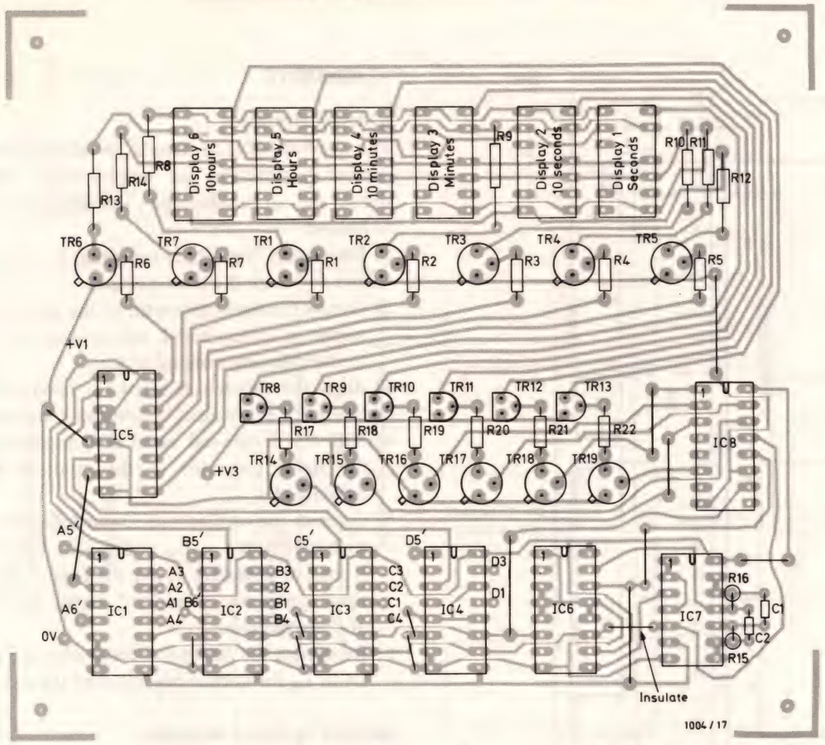


Fig.17 — Component layout of printed-wiring board 3, comprising multiplexing and driving circuits and six common-anode 7-segment LED displays (actual size)

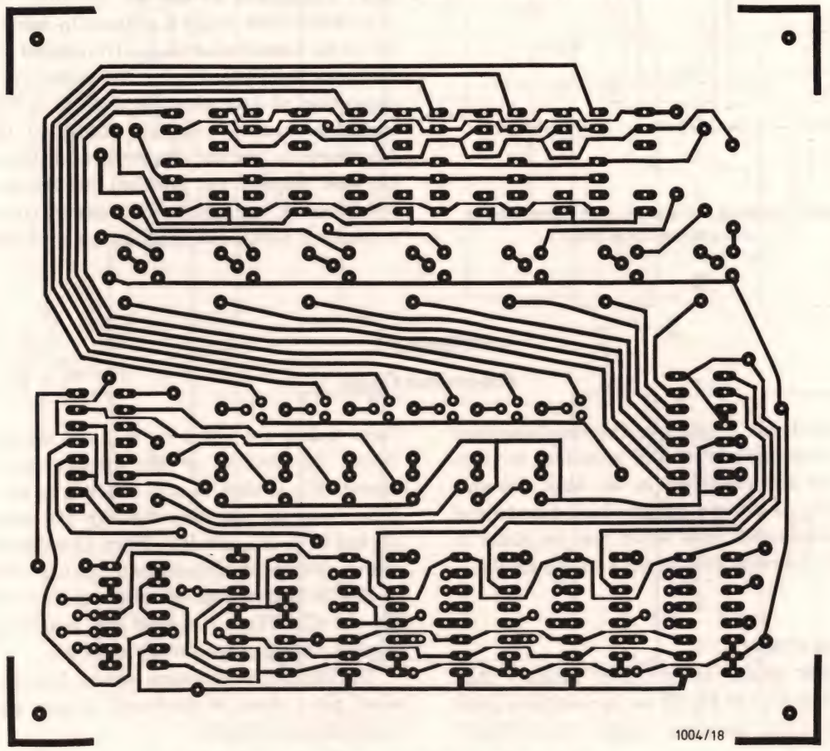


Fig.18 — Copper side of printed-wiring board (actual size)

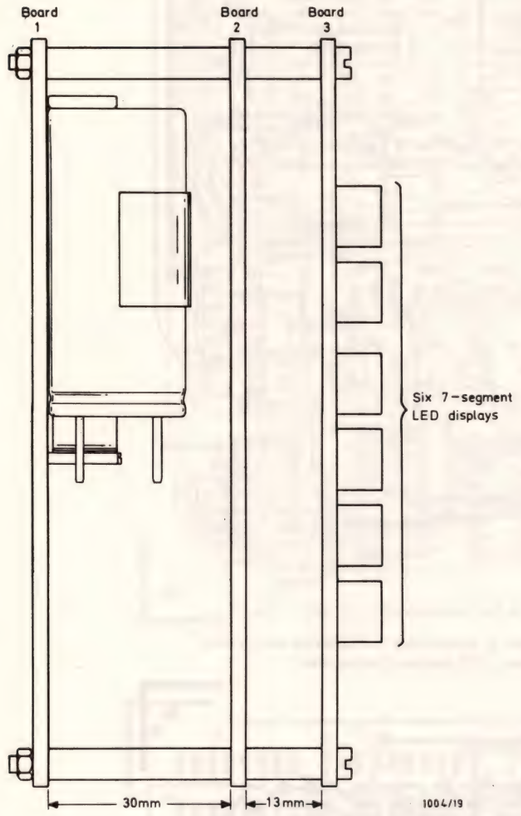


Fig.19 — Suggested mounting and spacing of the three printed-wiring boards (plan view)

ALIGNMENT

Receiver alignment

The receiver (Fig.5) should be aligned using a signal generator, providing an unmodulated 60kHz output signal, and an oscilloscope. The alignment procedure is as follows.

1) Disconnect the ferrite-rod aerial (comprising L_1, C_1, and C_2) from the receiver input.
2) Couple the signal generator to the ferrite-rod aerial by means of a loop aerial, and connect the oscilloscope to the coupling winding of L_1.
3) Align the ferrite-rod aerial for maximum output at 60kHz by adjustment of trimmer capacitor C_2.
4) With the ferrite-rod aerial still disconnected, couple the signal generator to the input of IC_1 through capacitor C_3.
5) Connect the oscilloscope to the collector of TR_1, and align inductors L_2, L_3, and L_4 for maximum output. It may be necessary to key the output signal from the signal generator on and off during the final peaking of these inductors.
6) Reconnect the ferrite-rod aerial after the alignment of L_2 to L_4 for normal operation of the receiver.

Decoder oscillator alignment

The crystal oscillator in the decoder circuit may require slight adjustment to set the operating frequency to 3.2768MHz. The circuit is adjusted by selecting a capacitor of the correct value for C_2. (A nominal value of 30pF is shown for C_2 in Fig.7.) For optimum speed in the acquisition of data after the clock is switched on, the oscillator should be within 200Hz of the specified frequency. In practice, however, once the minute data has been received, and provided that the circuit remains synchronised, the clock will operate correctly if the oscillator is within ±5kHz of the specified value.

APPENDIX 1
Add-on Date Circuit

The information (hours, minutes, and seconds) displayed by the radio clock can be extended to include the day-and-month data also contained in the MSF fast-code transmission. Fig.20 shows a circuit which decodes and displays this information, and which may be added to the clock without modification to the existing circuit.

CIRCUIT OPERATION

The 10ms clock pulses for the two auxiliary shift registers (IC_3 and IC_4) in Fig.20 are derived from point F (pin 3 of IC_{3A}) in the main decoder circuit (Fig.7). These pulses are gated by IC_1 and counted by IC_2. During the clocking of the minutes and hours data, counter IC_2 is reset to zero. Starting at the 'detect 41' pulse from the decoder, the day and month data is clocked in to IC_3 and IC_4. When 12 pulses are counted, further clocking is inhibited until the next minute.

The BCD data from the shift registers is decoded by IC_5 to IC_8. These ICs drive the common-cathode 7-segment LED displays directly as shown.

The laboratory prototype add-on date circuit is hard-wired on a sheet of pin-board to give the suggested layout shown in Fig.21.

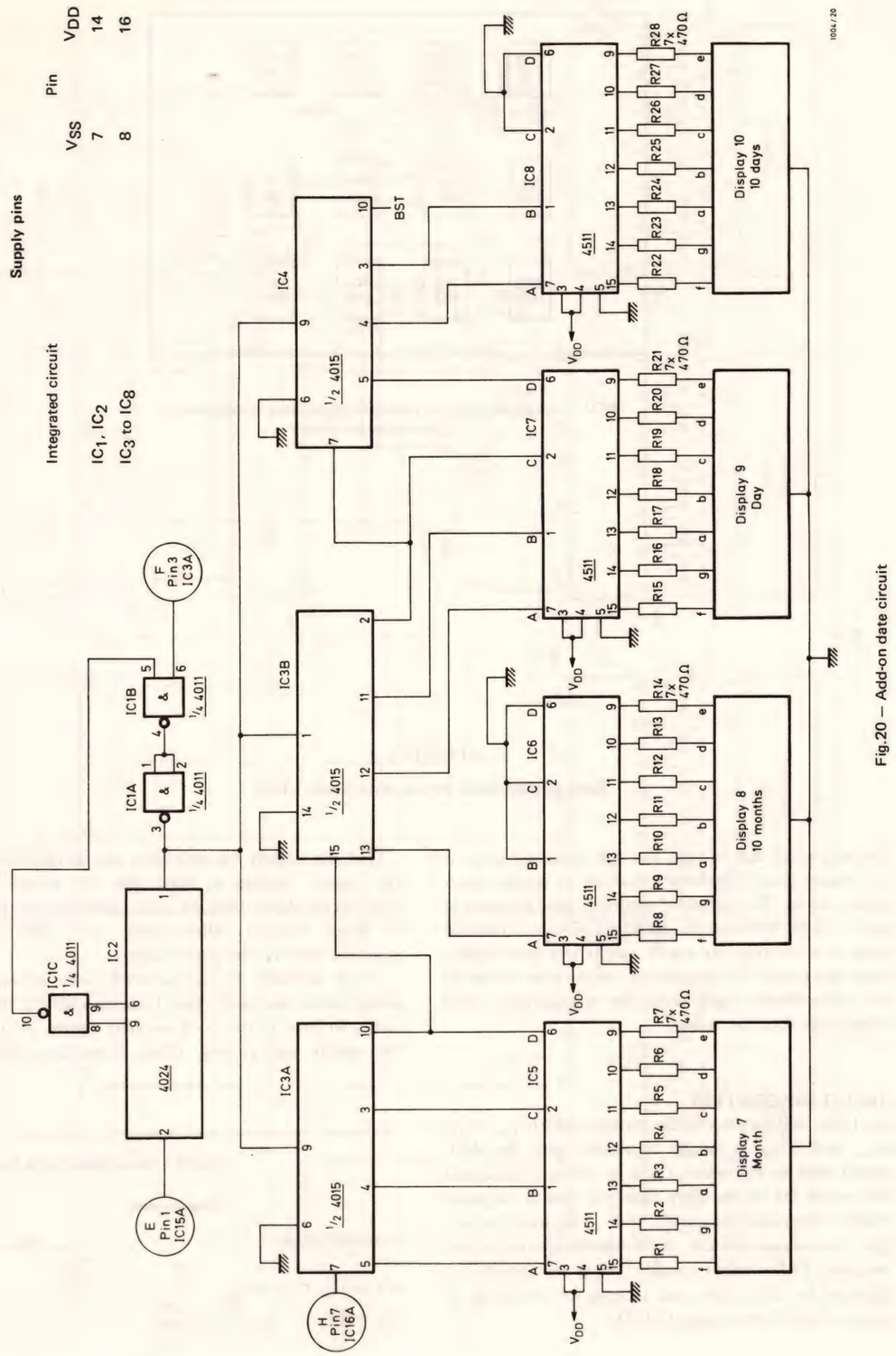


Fig.20 — Add-on date circuit

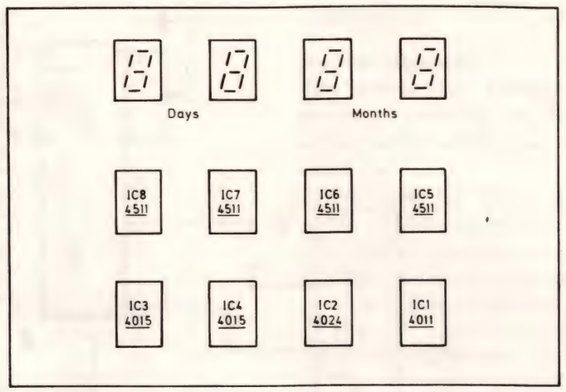


Fig.21 – Suggested layout of principal components of laboratory prototype date circuit

APPENDIX 2

Slave-display clock for use with Radio Clock

The radio clock can be used as a self-contained unit, or as a master clock supplying a number of remote slave-display clocks. The circuit of a suitable slave is shown in Fig.22. Where, for example, clocks are required in several rooms in a building, the use of master and slave-display clocks can reduce the component cost because, as can be seen from Fig.22, each slave has considerably fewer components than the master.

The d.c. supply for each slave can be obtained from the master, bearing in mind that the power supply (Fig.10) should be designed to accommodate the number of slaves required. Alternatively, each slave can be provided with its own power supply.

It is advisable to use screened cable between the master clock and each slave. Four-core cable is required, with two lines for the clock and data signals, and two for the supply and ground. (Only three lines would be

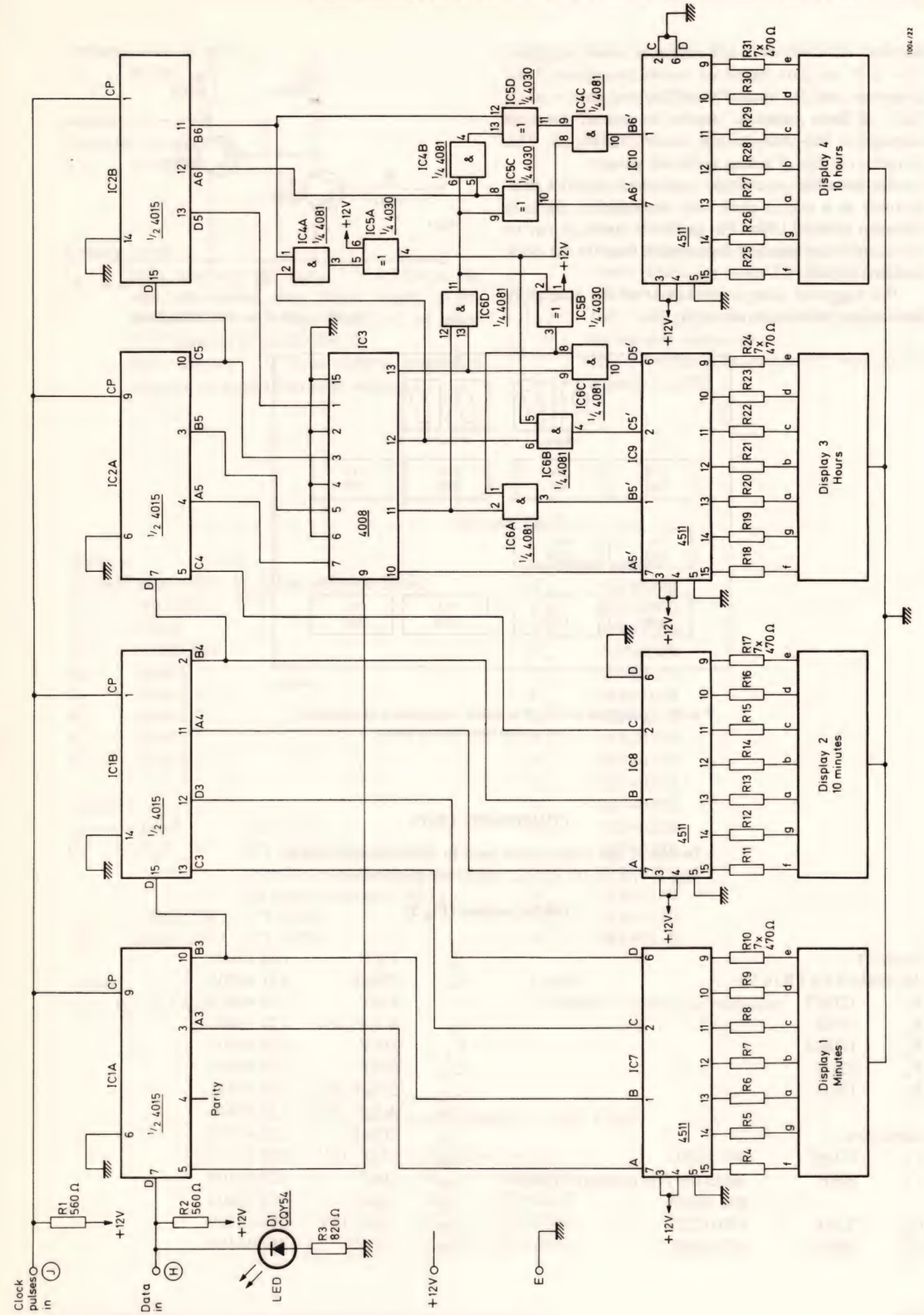
CIRCUIT DESCRIPTION

The 16-bit shift-register bank, consisting of IC_{1A}, IC_{1B}, IC_{2A}, and IC_{2B}, is loaded in parallel with the shift-register bank in the master clock by means of clock and data pulses fed to the slave from the master. Separate decoder integrated circuits IC_7 to IC_{10} are used for each digit, and these devices drive the common-cathode 7-segment LED displays directly. Hours and minutes are displayed by four digits, and seconds are indicated by pulses of light from a single LED D_1.

Fig.22 – Slave-display clock circuit ▷

Supply pins

Integrated circuit	Pin V_{SS}	Pin V_{DD}
IC_1 to IC_3, IC_7 to IC_{10}	8	16
IC_4 to IC_6	7	14



required for slaves with self-contained power supplies.) The clock and data signals are derived from points J and H in the decoder circuit (Fig.7) of the master clock. Each of these points is coupled to one of the lines through a line-driver circuit, shown in Fig.23. This circuit is capable of driving up to five slaves.

The laboratory prototype radio clock operates satisfactorily as a master clock with slave-display clocks at distances of up to 100m. For greater distances, it may be necessary to use matched transmission lines for the clock and data signals.

The suggested component layout of the laboratory slave-display clock is shown in Fig.24.

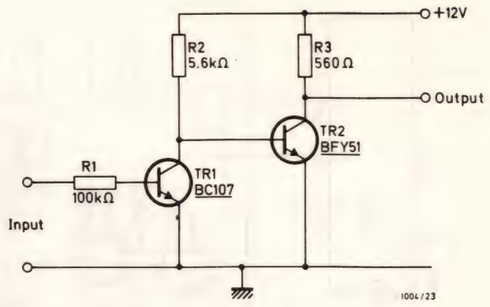


Fig.23 – Line driver for master clock

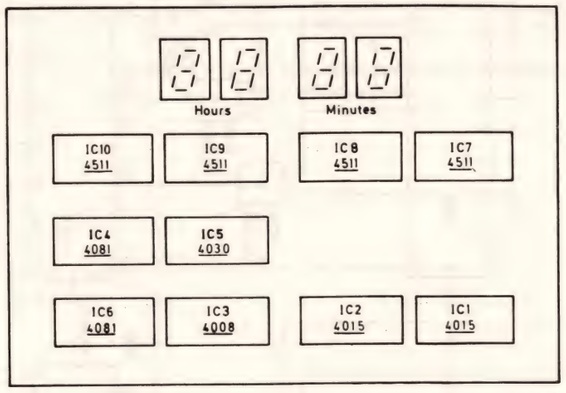


Fig.24 – Suggested layout of principal components of laboratory prototype slave-display clock

COMPONENT LISTS

Details of the components used in the circuits shown in Figs.5, 7, 8, 9, 10, 20, 22, and 23 are given below.

60kHz receiver (Fig.5)

Resistors
All resistors are CR16 5%

R_1	120kΩ	
R_2	390Ω	
R_3	180kΩ	
R_4	22kΩ	
R_5	10kΩ	

Capacitors

C_1	470pF	427 44701
C_2	60pF	Miniature film dielectric trimmer 808 32659
C_3	2.2nF	630 02222
C_4	390pF	427 43901
C_5	10pF	632 10109
C_6	390pF	427 43901
C_7	47nF	352 44473
C_8	4.7μF, 25V	122 56478
C_9	10nF	352 44103
C_{10}	47nF	352 44473
C_{11}	330μF, 4V	016 12331
C_{12}	4.7μF, 25V	122 56478
C_{13}	100nF	352 44104
C_{14}	15μF, 16V	015 15159
C_{15}	10nF	629 02103
C_{16}	5.6nF	425 45602
C_{17}	33μF, 16V	015 15339
C_{18}	100nF	352 44104

Transistor

TR_1	BC108

Integrated circuit

IC_1	TDA1050

Winding details

L_1 Main winding: 300 turns 7 X 0.125mm litz wire, pile-wound over 10mm length at the centre of 200 X 10mm ferrite rod of grade 4A10 material 4311 020 55470
Link winding: 10 turns 0.4mm enamelled copper wire wound over main winding.

L_2 Main winding: 366 turns 0.09mm enamelled copper wire
Link winding: 13 turns 0.18mm enamelled copper wire wound over main winding
10mm Vinkor pot-core LA1421 with standard adjuster LA1383

L_3 Main winding: 366 turns 0.09mm enamelled copper wire
Link winding: 6 turns 0.18mm enamelled copper wire wound over main winding
10mm Vinkor pot-core LA1421 with standard adjuster LA1383

L_4 100 turns 0.18mm enamelled copper wire, wound with centre-tap
10mm Vinkor pot-core LA1421 with standard adjuster LA1383

Decoder (Fig.7)

Resistors
All resistors are CR16 5% unless otherwise stated

R_1	1MΩ 10%
R_2	6.8kΩ
R_3	470kΩ 10%
R_4	100kΩ
R_5	100kΩ
R_6	100kΩ
R_7	220kΩ
R_8	100kΩ

Capacitors

C_1	100nF	122 57107
C_2	27pF	632 34279 in parallel with capacitor selected on test (nominal total capacitance 30pF)
C_3	2.2μF, 25V	122 56228
C_4	2.2μF, 25V	122 56228

Diodes

D_1 to D_9	BAW62

Integrated circuits

IC_1	HEF4049B
IC_2	HEF4020B
IC_3	HEF4518B
IC_4	HEF4068B
IC_5	HEF4013B
IC_6	HEF4518B
IC_7	HEF4011B
IC_8	HEF4024B
IC_9	HEF4013B
IC_{10}	HEF4081B
IC_{11}	HEF4049B
IC_{12}	HEF4082B
IC_{13}	HEF4082B
IC_{14}	HEF4082B
IC_{15}	HEF4013B
IC_{16}	HEF4015B
IC_{17}	HEF4015B

Crystal
3.2768MHz series-mode resonance

GMT-to-BST converter circuit (Fig.8)

Integrated circuits

IC_{18}	HEF4081B
IC_{19}	HEF4081B
IC_{20}	HEF4030B
IC_{21}	HEF4008B

Display circuit (Fig.9)

Resistors
All resistors are CR16 5% unless otherwise stated

R_1 to R_7	1kΩ
R_8 to R_{14}	see under 'Display'
R_{15}	100kΩ
R_{16}	100kΩ
R_{17} to R_{22}	680Ω

Capacitors

C_1	3.3nF	630 02332
C_2	3.3nF	630 02332

Transistors

TR_1 to TR_7	BC109
TR_8 to TR_{13}	BC328
TR_{14} to TR_{19}	BC109

Integrated circuits

IC_1 to IC_4	HEF4051B
IC_5	HEF4511B
IC_6	HEF4516B
IC_7	HEF4011B
IC_8	HEF4028B

Displays

Display 1 to 6	CQY81

Power supply (Fig.10)

Capacitor

C_{19}	4700μF, 16V	071 15472

Diodes

D_1	BY164
D_2	BY164

Transformer
Secondary windings 4 and 10V r.m.s.

Add-on date circuit (Fig.20)

Resistors

R_1 to R_{28}	470Ω	CR25 5%

Integrated circuits

IC_1	HEF4011B
IC_2	HEF4024B
IC_3	HEF4015B
IC_4	HEF4015B
IC_5 to IC_8	HEF4511B

Displays
Display 7 to 10 common-cathode 7-segment LED displays

Slave-display clock circuit (Fig.22)

Resistors
All resistors are CR25 5%

R_1	560Ω
R_2	560Ω
R_3	820Ω
R_4 to R_{31}	470Ω

LED

D_1	CQY54

Integrated circuits

IC_1	HEF4015B
IC_2	HEF4015B
IC_3	HEF4008B
IC_4	HEF4081B
IC_5	HEF4030B
IC_6	HEF4081B
IC_7 to IC_{10}	HEF4511B

Displays
Display 1 to 4 common-cathode 7-segment LED displays

Line driver for master clock (Fig.23)

Resistors
All resistors are CR25 5%

R_1	100kΩ
R_2	5.6kΩ
R_3	560Ω

Transistors

TR_1	BC109
TR_2	BFY51

ACKNOWLEDGEMENT
The authors would like to thank B.R. Swabey of the Division of Electrical Science, National Physical Laboratory, Teddington, UK, for his assistance with this article.

Mullard Technical Communications, Vol.14, No.139, July, 1978

The safe operation of power transistors
On pages 355 and 356, the symbols $M_{SB(I)}$ and $M_{SB(V)}$ were incorrectly defined. The correct definitions are:

$M_{SB(I)}$ = the multiplying factor at *constant current* = *voltage* multiplying factor, and

$M_{SB(V)}$ = the multiplying factor at *constant voltage* = *current* multiplying factor.

Therefore, in the above article, for $M_{SB(V)}$ read $M_{SB(I)}$, and for $M_{SB(I)}$ read $M_{SB(V)}$. Note that this affects Figs.20 and 21 as well as the text on pages 355 and 356; however, the actual values in Example 4 are correct.

A sample-and-hold balancing and protection circuit for push-pull switched-mode power supplies

L.E. JANSSON
Mullard Application Laboratory

This article discusses how the full capabilities of a push-pull switched-mode power supply may be realised, using the waveform generator, control, and protection circuit described. The circuit incorporates a novel sample-and-hold section that protects the output transistors against destruction due to unbalanced conduction. It also includes sections to prevent simultaneous conduction in the output transistors, to ensure that the drive pulses are of sufficient amplitude, to limit the output current, and to ensure that the protection circuits continue to operate under transient conditions. To illustrate the capabilities of the circuit, its performance in a 500W push-pull switched-mode power supply is described.

INTRODUCTION

Where a power supply is required to provide large currents at low voltage, the preferred choice in many cases is a push-pull switched-mode supply because such a supply offers the prospect of minimum ripple and the smallest output transformer and choke.

Push-pull switched-mode power supplies are, however, liable to flux imbalance and saturation in the output transformer, causing the destruction of the output transistors. Such imbalance may be caused by imperfectly matched output transistor storage times or unequal bottoming voltages, an unstable voltage feedback loop, rapid load current switching, or switching-frequency pick-up by the voltage feedback loop. To overcome the tendency to imbalance, a system is needed to balance the currents in the output transistors. In the past, such systems have used a balancing signal that is the integrated difference between signals that are proportional to the output transistor currents. However, since these systems are inherently time-averaging, they may fail to respond to rapidly changing operating conditions and therefore may not provide sufficient protection for the output transistors.

In the sample-and-hold balancing circuit described (patent applied for), however, the output transistor current in each half-cycle of operation is compared with, and controlled by, the current in the other transistor during the preceding half-cycle. This system prevents the current in one transistor exceeding that in the other by more than a small amount. Therefore, the flux excursion in the output transformer is restricted under both steady-state and transient operating conditions.

IMBALANCE IN PUSH-PULL SWITCHED-MODE POWER SUPPLIES

In discussing the imbalance of currents in a push-pull switched-mode power supply, it is helpful to consider the output stage illustrated in Fig.1. Under steady-state conditions, and where the output transistors are closely

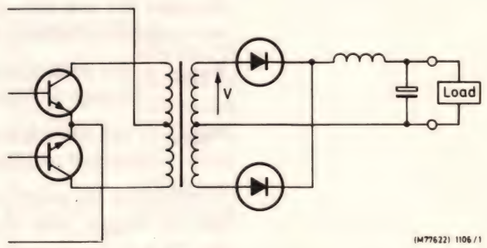


Fig.1 — Output stage of a push-pull switched-mode power supply

matched, the secondary voltage V and magnetising current I_{mag} in the output transformer will be as illustrated in Fig.2a. It can be seen that the average magnetising current $I_{mag(av)}$ is zero.

The variation of I_{mag} shown in Fig.2a can be explained as follows. When the first transistor is conducting, V is positive and I_{mag} increases linearly from its maximum negative value at the start of the conduction period to its maximum positive value at the end of the conduction period. (At the mid-point of the conduction period I_{mag} passes through zero.) When the second transistor is conducting, V is negative and I_{mag} decreases. When neither transistor is conducting, both output rectifiers are held in the conducting state by the output choke current, which is normally much greater than the transformer magnetising current. During the period when neither transistor is conducting and both output rectifiers are conducting, the transformer secondary is effectively short-circuited and so V is zero. Consequently (because the rate of change of magnetising current is proportional to the e.m.f.), the rate of change of the transformer magnetising current is zero; that is, I_{mag} remains at either its maximum positive or maximum negative value while both transistors are non-conducting.

If the conduction times of the two output transistors are unequal, as illustrated in Fig.2b, it can be seen that $I_{mag(av)}$ gradually increases (the transformer core magnetisation is said to 'staircase'), terminating in saturation of the transformer and destruction of the output transistors. Similarly, unequal bottoming voltages of the output transistors can produce saturation, as illustrated in Fig.2c. The same effect can be caused by switching-frequency pick-up in the voltage feedback loop, an unstable voltage feedback loop, or rapid load current switching as illustrated in Fig.3.

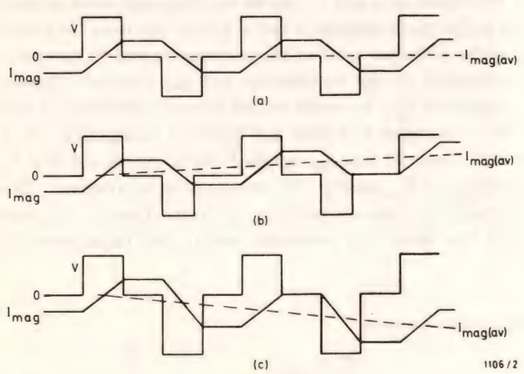


Fig.2 — Output transformer secondary voltage and magnetising current versus time:
(a) ideal steady-state conditions
(b) unequal conduction times in output transistors
(c) unequal bottoming voltages in output transistors

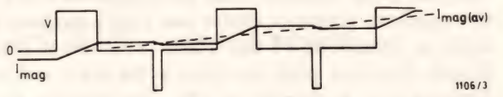


Fig.3 — Flux 'staircasing' due to switching-frequency signal in the voltage feedback loop

THE SAMPLE-AND-HOLD BALANCING SYSTEM

The sample-and-hold balancing system operates by 'storing' a voltage proportional to the collector current of one of the output transistors in one half-cycle. The collector current of the other output transistor is then monitored during the following half-cycle and, if it exceeds the stored level, a signal is generated to terminate the base drive.

The signal fed to the balancing system from the output transistors is proportional to the collector currents, as shown in Fig.4. Following an initial turn-on

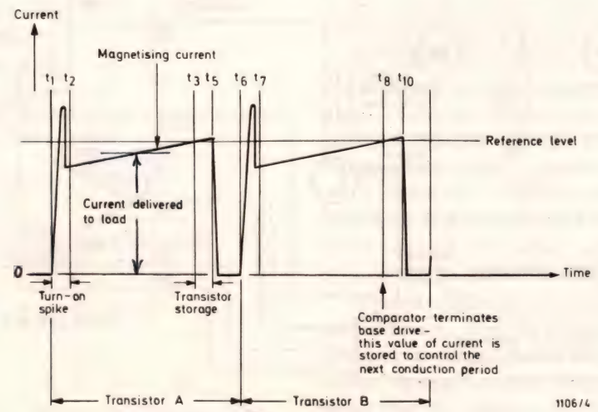


Fig.4 — Collector currents in the output transistors

spike, the signal can be considered to be a rectangle, whose height is proportional to the current delivered to the load, plus a linear ramp due to transformer and choke magnetising current.

Practical circuit

The operation of the sample-and-hold balancing system is now described with reference to Figs.5, 6, and 7. Fig.5 depicts the power output stage in outline, the waveform generator and control circuit as a block, and the sample-and-hold circuit in detail. The component numbers and connection numbers (shown circled in the figures) are the same as those used in the block diagram Fig.9 and in the complete circuit diagram Fig.10, shown later. Figs.6 and 7 are timing diagrams for the operation of the circuit.

At time t_1 in Fig.6 the drive pulse, on connection 12, causes the first output transistor to start conducting. When the initial switch-on spike has finished, at time t_2, the waveform generator circuit (see Fig.5) produces a signal on connection 17 that closes switch IC15b (and IC15c). Therefore point A, which is the lower end of capacitor C_{12}, is clamped to +5V. The capacitor C_{12} then charges rapidly to a potential equal to the difference between 5V and the voltage on connection 19, because the time-constant of capacitor C_{12} and associated resistances (that is, resistor R_{47} and the 'on' resistance of switch IC15b) is less than 100ns. Until time t_3 switch IC15b remains closed, the voltage at A remains at 5V, and the potential difference across capacitor C_{12} is determined by the current sense signal on connection 19. At time t_3 the waveform generator circuit terminates the drive pulse on connection 12 to the first output transistor, and open-circuits switch IC15b. The waveform generator circuit is designed so that, at time t_3, switch IC15a is also open-circuit. The charge on capacitor C_{12} therefore remains constant and the voltage at point A follows the signal on connection 19, as shown in Fig.6.

At time t_6 the drive pulse, on connection 13, causes the second output transistor to start conducting. When the initial switch-on spike has terminated, at time t_7, the waveform generator circuit produces a signal on connection 18 that closes switch IC15a to connect point A to the comparator. Thus the signal at C, which is applied to the comparator IC13b, becomes identical to the signal at A. At time t_7 the signal at 19, and therefore the signals at A and C, will be less than they were at time t_3. Therefore, signals A and C will be less than 5V which is the reference level of the comparator and so the input transistor of the comparator will not conduct, causing capacitor C_{12} to retain its full charge and signals A and C to continue to follow the signal on connection 19. A little later, at time t_8, signals A and C rise to and start to exceed 5V, causing the comparator to respond. The signal from the comparator, on connection 25, is taken to the waveform generator circuit and terminates the

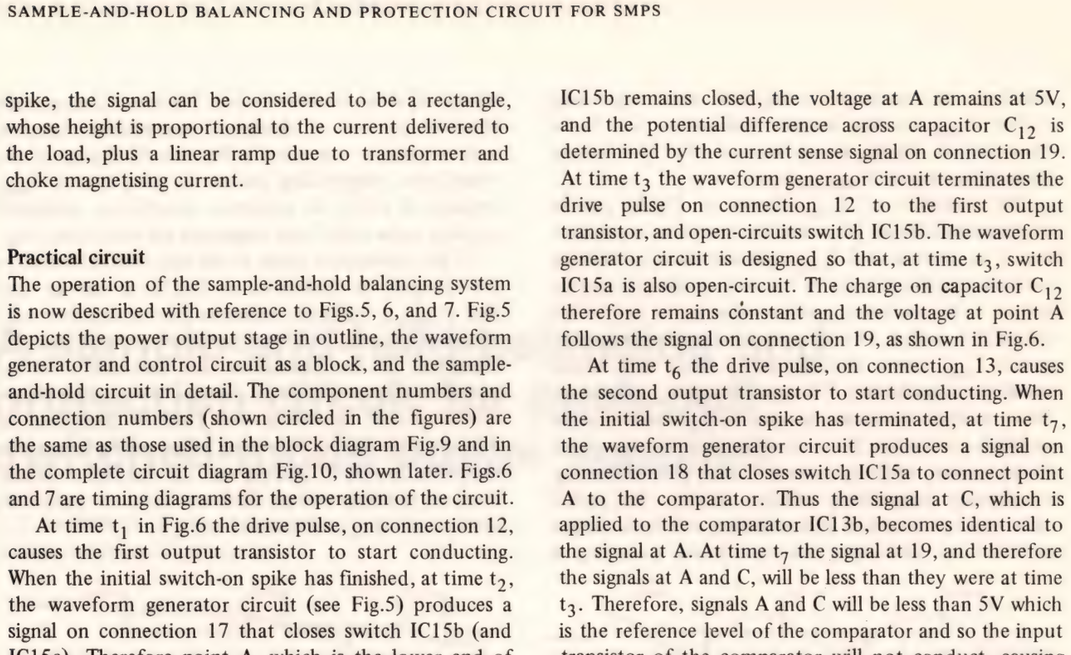
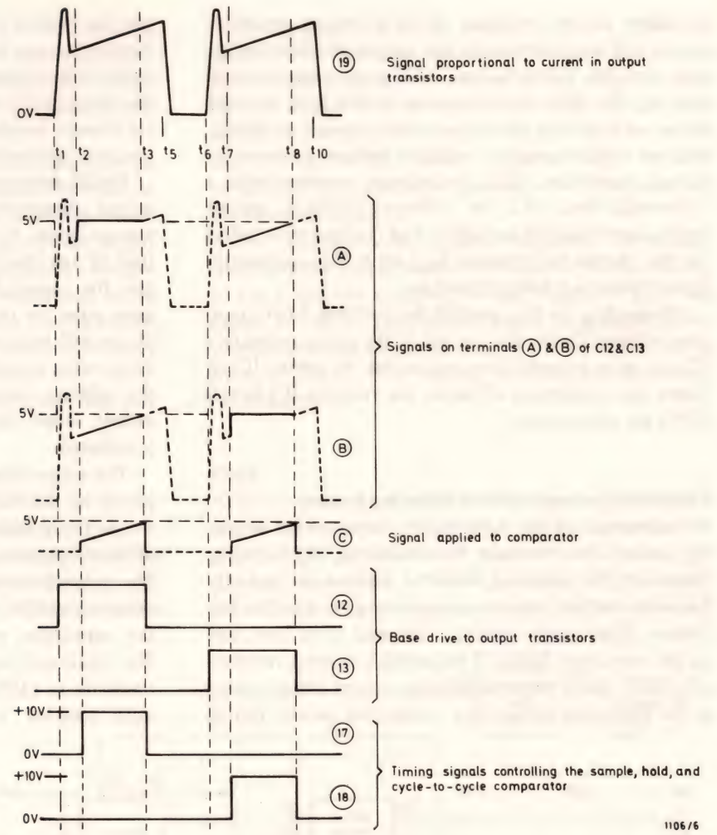


Fig.5 — Sample-and-hold balancing system

Fig.6 — Waveforms associated with the operation of the sample-and hold balancing system



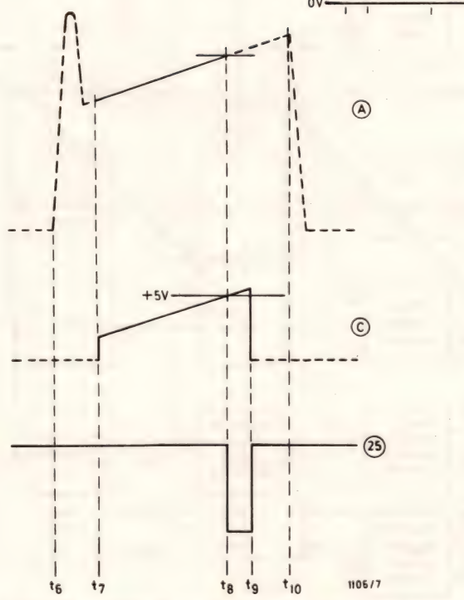


Fig.7 — Expanded waveforms to illustrate the operation of the level detector

second output transistor base drive. It should be noted that the output transistor current at time t_8, when the base drive is removed, is the same as the current at time t_3, which is when the base drive to the first output transistor was removed. Therefore the output transistor collector currents are equal.

The actions of the capacitor C_{13} and the switches IC15c and IC15d are identical to those described above except that while capacitor C_{12} is charging, capacitor C_{13} is driving the comparator, and vice-versa. Hence the signal at point B is similar to that at A but displaced by a half-cycle. There is therefore a continual comparison and balance of the output transistor collector currents.

To ensure that the sample-and-hold circuit stores the value zero if, for example, a drive pulse is missing, the circuit samples the output current for a minimum of 0.5μs (after the 2μs switch-on spike period).

Obviously, if the circuit described above maintained a perfect balance, then the output current from the supply would never change (in fact it would never switch on) to satisfy varying demand. Reference to Fig.7, however, shows that the signal at point C continues to rise for a short time between times t_8 and t_9. This occurs because

of delays in the operation of the waveform generator circuit and imperfections in the sample-and-hold circuit, such that the transistor base drive is not removed until time t_9. The delay between times t_8 and t_9 is arranged to be sufficient to allow the output current to change, and yet small enough to maintain balance between the output transistors. The comparator operates with a differential input of a few millivolts (<10mV), and its input current is small enough (<1μA) to have little effect on the charge in capacitor C_{12} while the comparator input transistor is being turned on.

Diodes D_{18} to D_{22} protect the switches from excessive voltages. Under the control of the clamp pulses (see 'Clamp pulse extender') on connection 16, switch IC12b biases the comparator off while the switches IC15a and IC15c are open-circuit.

Theoretical accuracy of the balancing system

An assessment of the theoretical accuracy of the balancing system can be made by considering Fig.8. Fig.8a represents the idealised collector current in perfectly balanced output transistors operating at 25kHz. The output choke ripple current is assumed to be zero, and so the waveform depicts a magnetising current variation of ±100% about zero magnetising current which occurs at the mid-point of the 20μs conduction period. During the first half of the conduction period, the magnetising current reduces the output transistor current below the reflected-load current represented by the 0% line. During the second half of the conduction period, the magnetising current increases the output transistor current above the reflected-load current.

Fig.8b represents the collector currents in a pair of output transistors having a 2μs difference between their storage times. For the output transistor with a storage time of 1μs, the drive pulse will terminate after 19μs to give the required total conduction time of 20μs. The drive pulse for the output transistor with a storage time of 3μs will be terminated by the balancing system after 17μs, when its collector current amplitude is identical to the collector current of the first output transistor at the instant when the drive pulse to that transistor was terminated.

The magnetising current at the end of the conduction period of the first output transistor is 90% of that for the perfectly balanced condition because the rate of rise of the magnetising current is constant at 100% per 10μs. The reduced maximum value of the magnetising current then reduces the output transistor current at the start of the conduction period of the second output transistor. The maximum value of the current in the second output transistor is 110% because the rate of rise of current is again constant. This increased maximum current in the second output transistor results in the −110% starting current of the first output transistor. Therefore, there will be a magnetising current and flux excursion in the output transformer 10% greater than that encountered under perfectly balanced conditions.

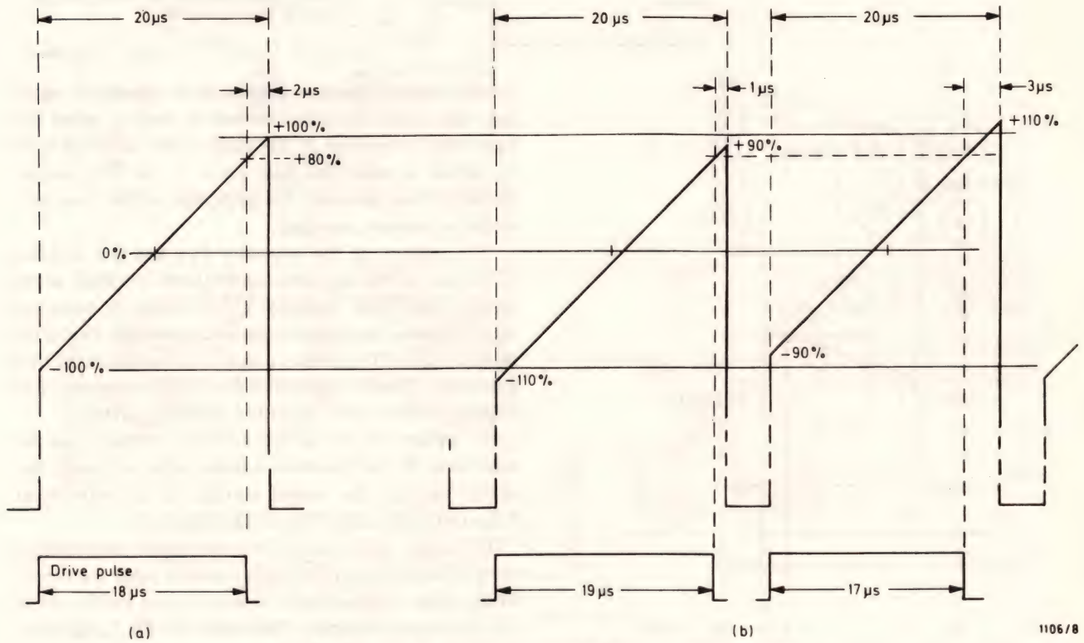


Fig.8 — Theoretical collector currents at 25kHz switching frequency:
(a) matched output transistors, with t_s = 2μs (b) unmatched output transistors, with t_{s1} = 1μs and t_{s2} = 3μs

The assumed figure of 2μs for the difference between the storage times represents the maximum that might be expected for high-voltage high-current switching transistors such as the BUX80 series. Thus, in a power supply incorporating a pair of these transistors and this sample-and-hold balancing system, the minimum design of the output transformer needs to allow for a flux excursion only 10% above that required for perfectly balanced operation. In practice, this margin may need to be increased by other factors that are discussed later (see 'Performance').

A COMPLETE WAVEFORM GENERATOR, CONTROL, AND PROTECTION CIRCUIT

The sample-and-hold balancing system already described may be incorporated into a complete waveform generator, control, and protection circuit as indicated in the block diagram Fig.9. In addition to the balancing function, the complete circuit incorporates sections to prevent simultaneous conduction in the output transistors, to ensure that the drive pulses are of adequate amplitude, to limit the output current, and to ensure that the protection circuits operate under transient conditions. The circuit also generates the drive pulses for the output transistors.

The waveforms on various numbered connections (circled in the figures) between the circuit blocks, shown in Fig.9 and the complete circuit diagram Fig.10, are shown in Fig.11. An outline circuit for a 500W power output stage and its connections to the control circuit is given in Fig.12. The various parts of the circuit are described below.

Clock

A linear sawtooth waveform, with an amplitude of 5V and a duration of 19.5μs (for 25kHz operation), is generated in the clock and applied to the modulator through connection 1. A delay, which is 0.5μs under normal operating conditions, is provided between each

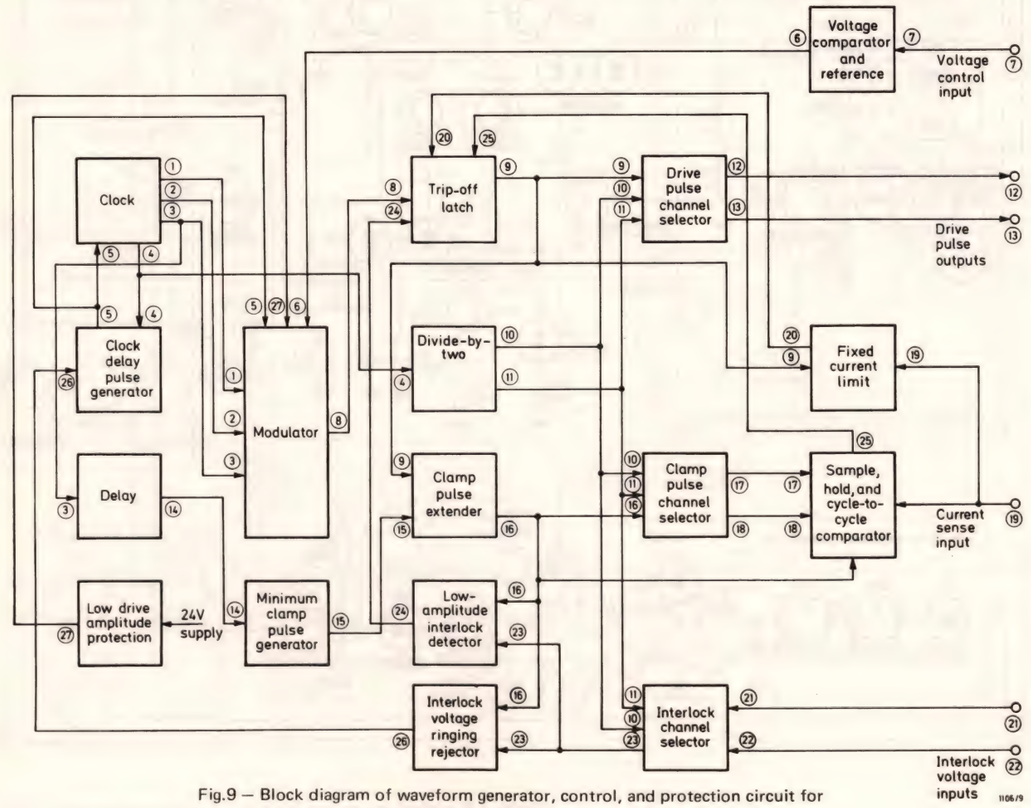


Fig.9 — Block diagram of waveform generator, control, and protection circuit for push-pull switched-mode power supplies

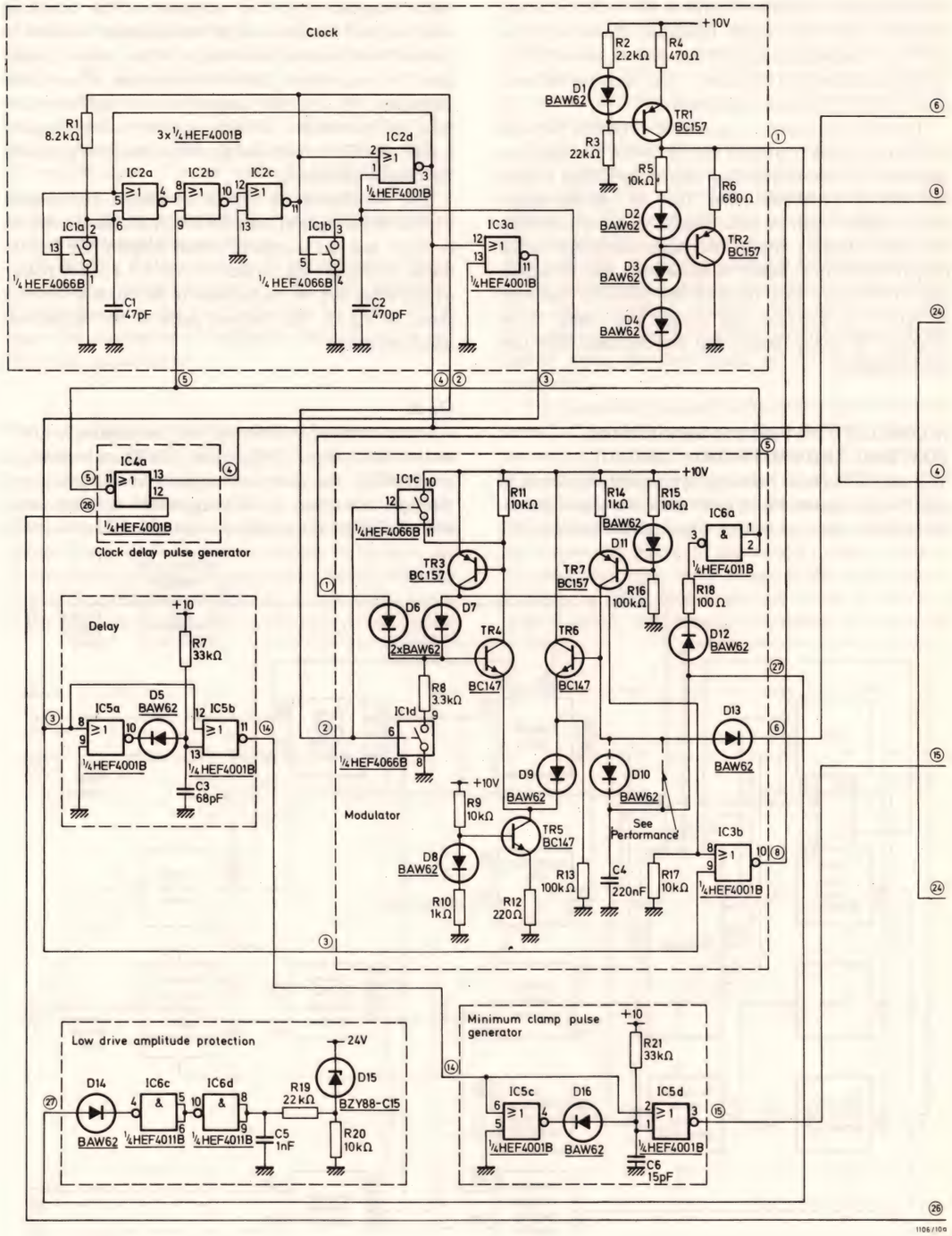
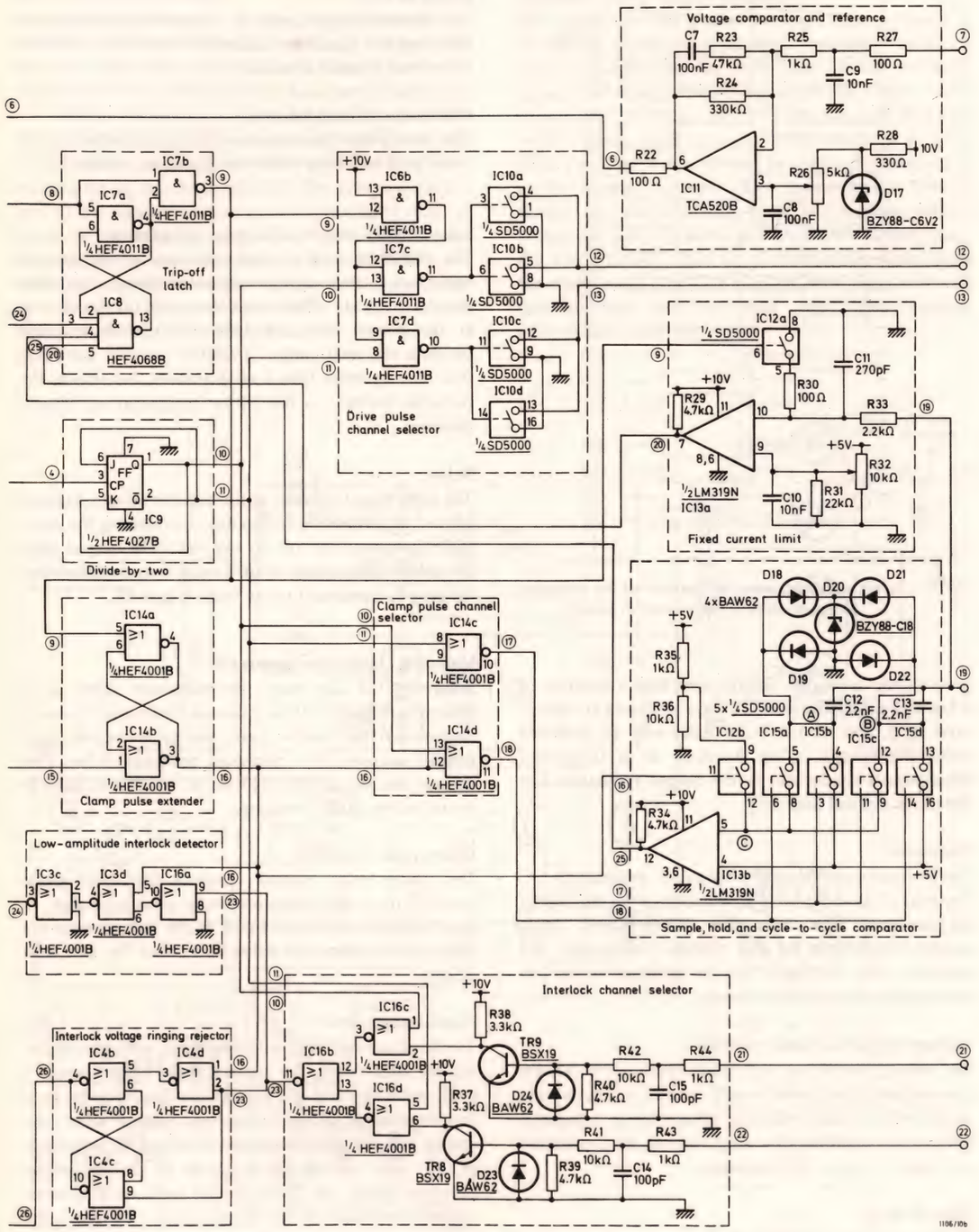


Fig.10 — Complete waveform generator, control, and protection circuit



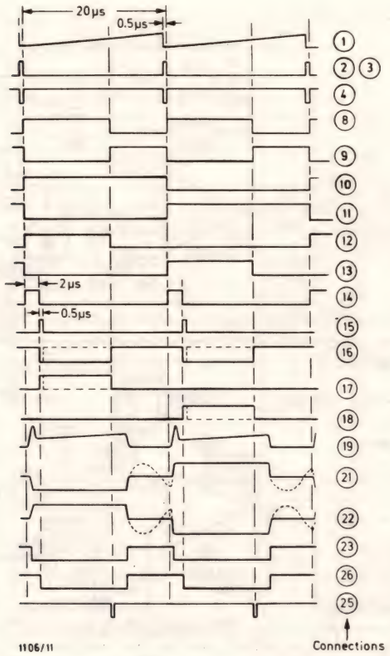


Fig.11 — Signals associated with the operation of the waveform generator, control, and protection circuit

cycle of the sawtooth. Squarewaves with a duration of 0.5μs and an amplitude of 10V are generated at connections 2, 3, and 4. The 0.5μs delay may be extended under the control of the interlock, so as to prevent simultaneous conduction in the output transistors (see 'Interlock channel selector').

Modulator
The modulator provides the drive pulses on connection 8. The start of the drive pulse is coincident with the start of the sawtooth. The drive pulse is terminated, under normal conditions, by the voltage comparator and reference. The modulator may be inhibited by the low drive amplitude protection circuit.

Voltage comparator and reference
The voltage comparator and reference circuit is entirely conventional. The power supply output voltage is compared with a stable reference voltage by an integrated operational amplifier. The output signal, on connection 6, is used to control the modulator.

Trip-off latch
The trip-off latch inhibits the output transistor drive pulses, in response to control signals received from the protection circuits.

Divide-by-two
The divide-by-two circuit is a conventional flip-flop, providing the signals on connections 10 and 11 to drive the various channel selectors.

Drive pulse channel selector
The drive pulse channel selector produces the conventional push-pull drive pulses for the output transistors.

Sample, hold, and cycle-to-cycle comparator
The principles and detailed operation of the sample, hold, and cycle-to-cycle comparator circuit have been discussed already. The circuit stores the output current at the instant that the drive pulse terminates, and prevents the next output transistor current exceeding this value by more than a small amount. In this way the collector currents in the output transistors are closely balanced.

Delay
The delay circuit operates at the negative-going transition of the clock signal on connection 3, producing the delay pulse on connection 14. To suit the 500W output stage the delay is 2μs, which is sufficiently long to ensure that the output transistor turn-on spike is ignored.

Minimum clamp pulse generator
Following the 2μs delay, the minimum clamp pulse generator produces a 0.5μs pulse on connection 15 which ensures that the sample, hold, and cycle-to-cycle comparator operates for a minimum period of 0.5μs. This ensures that the sample-and-hold circuit stores the value zero if a drive pulse is missing.

Clamp pulse extender
The clamp pulse extender extends the clamp pulse received from the minimum clamp pulse generator, so that the clamp pulse terminates at the same time as the drive pulse (unless the drive pulse lasts for less than 2.5μs).

Fixed current limit
The fixed current limit is conventional, and operates the trip-off latch when the current sense input exceeds a predetermined value. To prevent the fixed current limit from operating during the current turn-on spike, the current sense input is integrated to reduce the amplitude of the spike. Retention of charge in the integration capacitor from one cycle to the next could lead to unstable operation of the current limit. Therefore, the capacitor voltage is clamped to zero during the gaps between drive pulses by the inverted drive pulse waveform on connection 9.

Interlock channel selector
Simultaneous conduction by the output transistors is prevented by monitoring their collector voltages and using the signal generated to delay the drive pulse to one output transistor until the other has ceased conducting. To maintain the isolation of the output from the mains input, the output transistor collector voltage is monitored via the output transformer secondary winding (a separate winding could also be employed). The state of conduction of the output transistors can be monitored either in terms of the collector voltage (as here), or in terms of the collector current. However, the latter method is not favoured because the output transistors can store charge and, therefore, may retain the ability to conduct even though the collector current is small.

Interlock voltage ringing rejector
The purpose of the interlock voltage ringing rejector is to prevent a false interlock signal extending the clock delay period beyond the usual 0.5μs. A false interlock signal could arise if the voltage across the output transformer were to fall to zero, ring negative, and then ring positive again, which could be falsely interpreted (if the ringing rejector were omitted) as continuing conduction in the output transistor. The circuit uses a bistable element that can be set only when the low clamp pulse is present on connection 16, and the bistable is reset when the low interlock signal on connection 23 ends. Since the clamp pulse starts 2μs after the drive pulse, and ends simultaneously with the drive pulse, false interlock information is rejected.

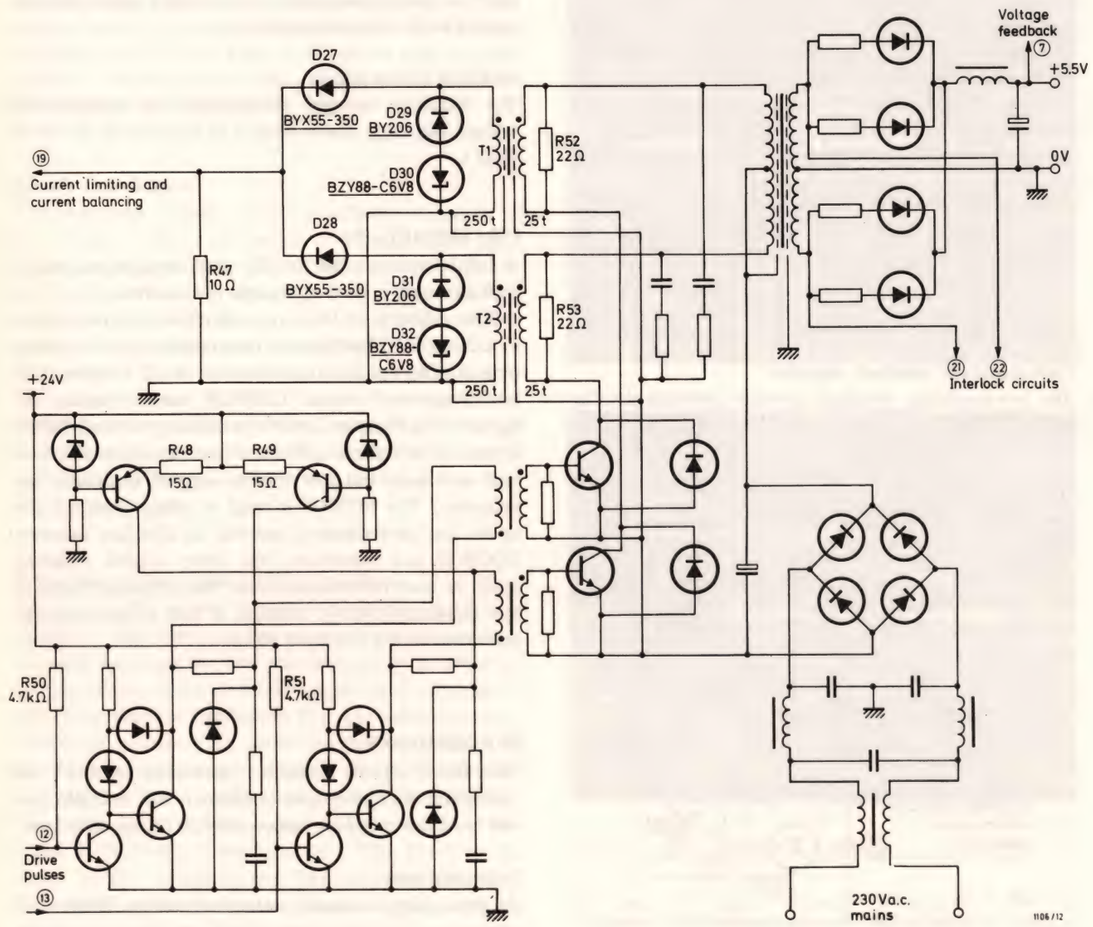


Fig.12 — Connections to a 500W push-pull output stage

In mains-operated power supplies, collector damping is usually necessary to prevent ringing so as to keep the output transistors within their safe operating areas when they are switched off and the mains supply is at its maximum. Ringing can, however, still occur when the mains voltage is reduced.

Clock delay pulse generator

The clock delay pulse generator extends the usual delay of 0.5μs between each cycle of the clock, during the time that a signal from the interlock voltage ringing rejector is present. The form of interlock used here ensures correct operation under all unusual conditions. For example, it is possible for an output transistor to have full base drive and negligible collector current, especially if the supply voltage is low, possibly causing the output transistor storage time to extend into (or exceed) the 20μs normally occupied by the next cycle of operation. (Inadequate base-charge extraction will increase the storage time.) The interlock method used here, which allows for a theoretically infinite storage time, protects the output transistors against simultaneous conduction irrespective of the operating conditions.

The clock delay pulse generator, as well as controlling the clock 'rest' period, is used to rapidly discharge capacitor C_4 in the modulator. This reduces the maximum allowable drive time, which then limits the extension of further clock delay pulses and maintains approximately constant-frequency operation.

Low-amplitude interlock detector

The low-amplitude interlock detector prevents simultaneous conduction occurring in the output transistors when the supply voltage is very low, in which case the interlock signal would be too small to operate the previously described protection circuits.

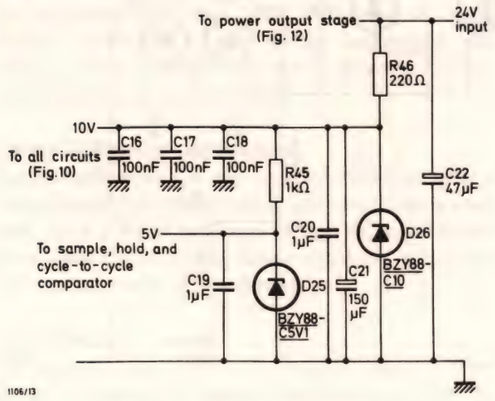


Fig.13 — Auxiliary power supplies

The low-amplitude interlock detector checks for the presence of an interlock signal on connection 23 two microseconds after the start of each drive pulse. The check is made by comparing the interlock signal with the clamp pulse on connection 16 which starts 2μs after the drive pulse. If an interlock signal is not present when the comparison is made, a signal is transmitted to the trip-off latch to terminate the drive pulse.

Low drive amplitude protection

If the output transistor base drive is too small to ensure saturation of the output transistors when the transistors are conducting their maximum collector currents, the base drive must be reduced to zero. The low drive amplitude protection circuit reduces the drive time to zero if the 24V auxiliary supply falls below 20V, ensuring that only drive pulses of sufficient amplitude are applied to the output transistors.

Auxiliary power supply

The auxiliary voltages are supplied by conventional voltage regulator diodes from a 24V input, as shown in Fig.13.

CIRCUIT DETAILS

A full component list for the waveform generator and control circuit is given at the end of this article.

The majority of the circuit functions are performed by LOCMOS HEF4000 series integrated circuits operating from a 10V supply. Transistors are used, however, for interfacing and where LOCMOS cannot readily be applied. The Signetics DMOS quad analog switch SD5000 is used in the sample-and-hold circuit, where its very low 'on' resistance and low feedthrough of transients are necessary. The SD5000 is used in other parts of the circuit for convenience to provide an interface between LOCMOS and transistors, but other suitable switches could be used in these locations. The comparator used is the Signetics LM319, because it has a fast response combined with a low input current.

PERFORMANCE

The ability of the complete circuit to provide total protection for the output transistors, and to make output transistor matching unnecessary, is discussed below.

Balancing errors

As previously mentioned under the heading 'Theoretical accuracy of the balancing system', the accuracy of the balancing system will be degraded by factors such as timing errors and voltage sensing errors. Timing errors in

the practical circuit are negligible, since the LM319 comparator has a nominal response time of 80ns, the LOCMOS gates have a propagation delay of 20ns (at 10V), and the SD5000 switches operate in less than 1ns.

Voltage sensing errors are more significant than timing errors, but are nevertheless small. The current monitoring resistor, R_{47} in Fig.12, generates a signal of 1V for 1A of collector current, and the ±100% change of magnetising current in Fig.8 corresponds to a voltage change of approximately ±100mV. Therefore, assuming that the input current of the LM319 is 250nA, and that this current is drawn for 18μs from the 2.2nF capacitors C_{12} and C_{13}, the resulting error is 2mV which corresponds to a 2% increase in flux excursion.

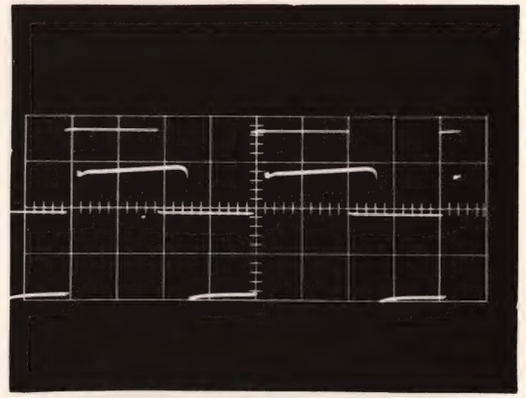
The typical input offset voltage of the LM319 is 2mV and the maximum value is 10mV, causing a typical increase in flux excursion of 2% and a maximum of 10%. This error can be removed by adjusting the input offset voltage with a potentiometer connected to the non-inverting input of the LM319. It can be seen that the accuracy of the system may, therefore, be made to approach the theoretical limit.

Steady-state balance

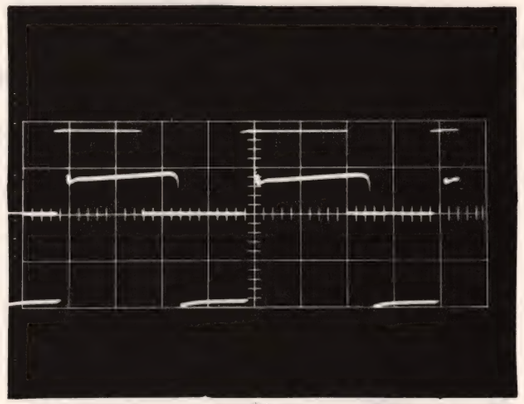
The measured output transistor collector currents, in Fig.14, show that a difference of storage times t_s of 1.5μs has little effect. (The difference of 1.5μs was artificially induced by replacing resistors R_{48} and R_{49} in Fig.12, with 10Ω resistors joined by a 10Ω potentiometer. The potentiometer was adjusted to produce a difference of 2:1 in the output transistor base currents.) The measurements published here were made at an output power of 500W. However, measurements at all load currents from zero to maximum, and at all supply voltages, show that the balance is never worse than that depicted in Fig.14.

Protection against load-switching transients

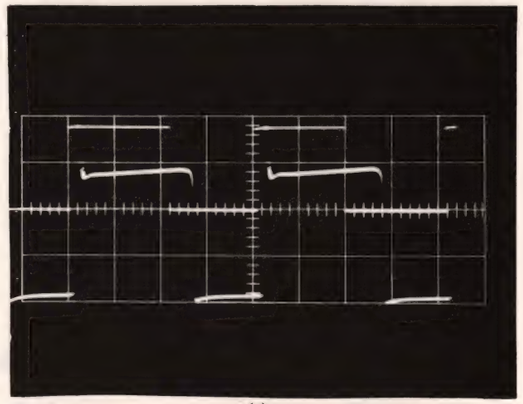
To protect the output transistors from any imbalance caused by false signals in the voltage feedback loop, it is normally necessary to limit the slew-rate at the input to the modulator. Such slew-rate limitation is provided in Fig.10 by the wire link across D_{10}. (In normal use D_{10} would be omitted.) To determine the performance of the balancing system under the most stringent conditions, the wire link was removed (so removing slew-rate limitation) and 1V of 25kHz squarewave derived from the divide-by-two circuit was used as a false signal to the input of the voltage-control feedback amplifier IC_{11}. This false signal produced a similar signal, with an amplitude of 4V, at the modulator input, causing one output transistor to conduct for the maximum time and the other to conduct for a short time. The observed



(a)



(b)



(c)

Fig.14 — Measured output transistor collector currents and drive pulse waveforms:
(a) $I_{b(left)} = I_{b(right)}$ $t_{s(left)} = 3\mu s$ $t_{s(right)} = 3\mu s$
(b) $I_{b(left)} = 2I_{b(right)}$ $t_{s(left)} = 4\mu s$ $t_{s(right)} = 2.5\mu s$
(c) $2I_{b(left)} = I_{b(right)}$ $t_{s(left)} = 2.5\mu s$ $t_{s(right)} = 4\mu s$
Vertical scale: 1A/div.
Horizontal scale: 5μs/div.

balance of the output transistor currents remained as good as that shown in Fig.14. The only observable effect was to reduce the power supply output to correspond with the lower of the input levels to the modulator.

The only limitation on the protection provided by the balancing circuit, without slew-rate limiting, is that it cannot switch off a drive pulse until after the end of the current turn-on spike (that is, 2μs after the start of the drive pulse, for the circuit values employed). To determine the effect of this limit to the protection, the drive to one transistor was disconnected and the supply was operated at maximum mains voltage, producing a 2μs drive pulse to one transistor and causing the output transformer to partially saturate. However, the transistor remained within safe operating conditions with load resistance values corresponding to the range of at least 0 to 80% of full load. In practice, with the slew-rate limiting operating, the maximum difference between successive drive pulses would be 0.5μs, giving safe operation with drive pulse lengths above and below 2μs.

The circuit provides protection for the output transistors against most forms of maladjustment and faulty operating conditions. Provided that the single current sense input (connection 19) is correctly connected, any or all of the drive, interlock, voltage control, and supply voltage connections can be open-circuited (being faults that could possibly occur in newly manufactured power supplies) without damage.

COMPONENT LIST

Waveform generator, control, and protection circuit (Fig.10)

Resistors

All resistors are CR16, 5% except where noted

R_1	8.2kΩ	
R_2	2.2kΩ	
R_3	22kΩ	
R_4	470Ω	
R_5	10kΩ	
R_6	680Ω	
R_7	33kΩ	
R_8	3.3kΩ	
R_9	10kΩ	
R_{10}	1kΩ	
R_{11}	10kΩ	
R_{12}	220Ω	
R_{13}	100kΩ	
R_{14}	1kΩ	
R_{15}	10kΩ	
R_{16}	100kΩ	
R_{17}	10kΩ	
R_{18}	100Ω	
R_{19}	22kΩ	
R_{20}	10kΩ	
R_{21}	33kΩ	
R_{22}	100Ω	
R_{23}	47kΩ	
R_{24}	330kΩ	
R_{25}	1kΩ	
R_{26}	5kΩ	preset potentiometer
R_{27}	100Ω	
R_{28}	330Ω	
R_{29}	4.7kΩ	
R_{30}	100Ω	
R_{31}	22kΩ	
R_{32}	10kΩ	preset potentiometer
R_{33}	2.2kΩ	
R_{34}	4.7kΩ	
R_{35}	1kΩ	
R_{36}	10kΩ	
R_{37}	3.3kΩ	
R_{38}	3.3kΩ	
R_{39}	4.7kΩ	
R_{40}	4.7kΩ	
R_{41}	10kΩ	
R_{42}	10kΩ	
R_{43}	1kΩ	
R_{44}	1kΩ	

Capacitors

C_1	47pF	632 34479
C_2	470pF	427 44701
C_3	68pF	632 34689
C_4	220nF	344 21224
C_5	1nF	425 41002
C_6	15pF	632 10159
C_7	100nF	344 21104
C_8	100nF	344 21104
C_9	10nF	344 51103
C_{10}	10nF	344 51103
C_{11}	270pF	632 58271
C_{12}	2.2nF	425 42202
C_{13}	2.2nF	425 42202
C_{14}	100pF	427 41001
C_{15}	100pF	427 41001

Diodes

D_1	BAW62	
D_2	BAW62	
D_3	BAW62	
D_4	BAW62	
D_5	BAW62	
D_6	BAW62	
D_7	BAW62	
D_8	BAW62	
D_9	BAW62	
D_{10}	BAW62	(used to remove slew-rate limiting when testing)
D_{11}	BAW62	
D_{12}	BAW62	
D_{13}	BAW62	
D_{14}	BAW62	
D_{15}	BZY88-C15 or BZX79-C15	
D_{16}	BAW62	
D_{17}	BZY88-C6V2 or BZX79-C6V2	
D_{18}	BAW62	
D_{19}	BAW62	
D_{20}	BZY88-C18 or BZX79-C18	
D_{21}	BAW62	
D_{22}	BAW62	
D_{23}	BAW62	
D_{24}	BAW62	

Transistors

TR_1	BC157
TR_2	BC157
TR_3	BC157
TR_4	BC147
TR_5	BC147
TR_6	BC147
TR_7	BC157
TR_8	BSX19
TR_9	BSX19

Integrated circuits

IC_1	HEF4066BP
IC_2	HEF4001BP
IC_3	HEF4001BP
IC_4	HEF4001BP
IC_5	HEF4001BP
IC_6	HEF4011BP
IC_7	HEF4011BP
IC_8	HEF4068BP
IC_9	HEF4027BP
IC_{10}	SD5000
IC_{11}	TCA520B
IC_{12}	SD5000
IC_{13}	LM319N
IC_{14}	HEF4001BP
IC_{15}	SD5000
IC_{16}	HEF4001BP

Auxiliary power supply (Fig.13)

Resistors

R_{45}	1kΩ	CR16 5%
R_{46}	220Ω	PR37

Diodes

D_{25}	BZY88-C5V1 or BZX79-C5V1
D_{26}	BZY88-C10 or BZX79-C10

Capacitors

C_{16}	100nF	344 21104
C_{17}	100nF	344 21104
C_{18}	100nF	344 21104
C_{19}	1μF	344 21105
C_{20}	1μF	344 21105
C_{21}	150μF, 25V	016 16151
C_{22}	47μF, 40V	016 17479

Power output stage (Fig.12)

The waveform generator, control, and protection circuit is designed for use with any push-pull switched-mode power output stage. Therefore only those components in the power output stage that are relevant to the operation of the waveform generator, control, and protection circuit are described.

Diodes

D_{27}	BYX55-350
D_{28}	BYX55-350
D_{29}	BY206
D_{30}	BZY88-C6V8 or BZX79-C6V8
D_{31}	BY206
D_{32}	BZY88-C6V8 or BZX79-C6V8

Resistors

R_{47}	10Ω	PR37
R_{48}	15Ω	PR37
R_{49}	15Ω	PR37
R_{50}	4.7kΩ	CR16 5%
R_{51}	4.7kΩ	CR16 5%
R_{52}	22Ω	PR37
R_{53}	22Ω	PR37

Transformers

T_1 and T_2 are identical current monitoring transformers of the following construction.

Core: Ferroxcube U-core type FX3605 with standard bobbin.

Windings:

1) 250 turns of 0.2mm diameter copper wire wound in 5 layers of 50 turns per layer, with 60μm Macrofol between layers;
2) 1 layer of 60μm Macrofol;
3) 0.05mm brass foil screen;
4) 3 layers of 60μm Macrofol;
5) 0.05mm brass foil screen;
6) 1 layer of 60μm Macrofol;
7) 25 turns of 0.4mm diameter copper wire in one layer;
8) 3 layers of 60μm Macrofol.

Product Information: Vision-i.f. ICS TDA2540 and TDA2541

INTRODUCTION

Two integrated circuits, types TDA2540 and TDA2541, provide the vision-i.f. and demodulator functions for colour or black-and-white tv receivers at an exceptional standard. The TDA2540 is intended for use with tuners requiring npn-polarity gain control, and the TDA2541 for tuners requiring pnp-polarity gain control.

The main benefits provided by these devices are given below.

Full i.f. amplification, combining high sensitivity with excellent stability.

Signal-to-noise ratio considerably better than that of the typical i.f. output signal of a tuner.
Negligible *intermodulation products* in the video output.

Large a.g.c. range, with an a.g.c. circuit that resumes control of the i.f. gain after the tuner a.g.c. has finished.

VCR (video cassette recorder) facility, inhibiting the video output signal of the receiver and providing a *high impedance* at the video output pin.

Sensitive a.f.c. circuit, giving a ±5V output swing over a range of only 100kHz.

A.F.C. inhibit facility for use during tuning.

White-spot and noise inversion circuits, to reduce the effect of interference on the picture.

TDA2540 AND TDA2541

The a.g.c. circuit of the TDA2540 provides a control current which *decreases* with increasing signal level. This output is suitable for tuners with an npn-polarity a.g.c. such as the U321, which requires a *decrease* in a.g.c. *current* for a reduction in gain. The a.g.c. output from the TDA2540 is also suitable for tuners with npn-polarity a.g.c. which require an *increase* in a.g.c. *voltage* for a reduction in gain.

The a.g.c. circuit of the TDA2541 provides a control current which *increases* with increasing signal level, this being suitable for tuners with a pnp-polarity a.g.c. such as the U322 and the V311, which both require a *decrease* in a.g.c. *voltage* for a reduction in gain.

As shown in the block diagram in Fig.1, the ICs contain the following circuit elements:

1) a gain-controlled wideband i.f. amplifier;
2) a synchronous demodulator with a low-distortion reference amplifier, giving a video signal containing negligible intermodulation products;
3) a noise-protected a.g.c. circuit, which resumes control of the i.f. gain after the tuner a.g.c. has finished;
4) a separate phase comparator for a.f.c., giving accurate and sensitive a.f.c., typically ±5V for a detuning of ∓50kHz;
5) a video preamplifier, providing a temperature-compensated output;
6) a VCR switch input, reducing the tuner and i.f. gain to a minimum and disabling the video preamplifier, thus giving a high output impedance at the video output pin for connection of a VCR;

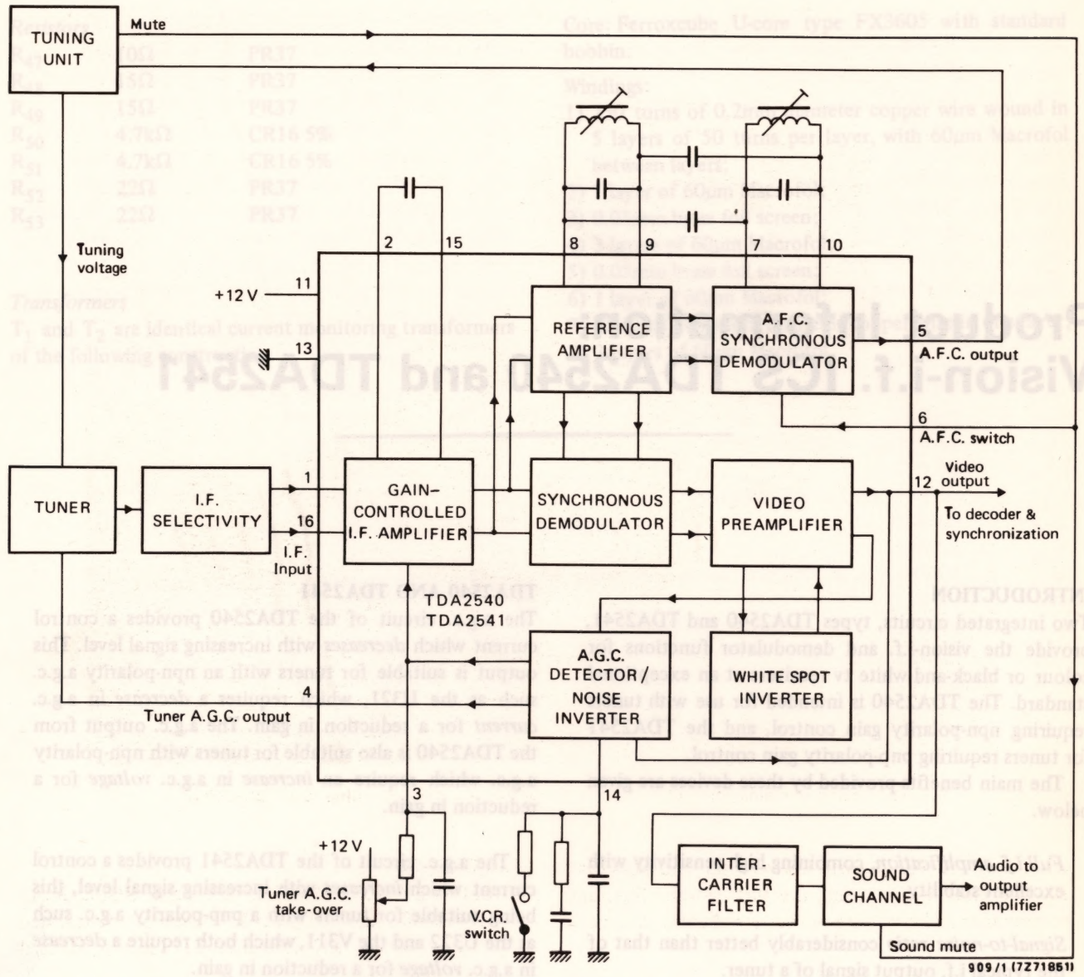


Fig.1 – Block diagram of the TDA2540 or TDA2541 and main peripherals

7) a white-spot inverter and a noise inverter to prevent ultra-white or black spots in the picture.

Full details of these circuit elements, and two practical r.f./i.f. receiver circuits, are given in Ref.1. Typical performance figures for both ICs are given below: further details are given in the published data for the TDA2540 and TDA2541.

I.F. gain control range	64dB
Signal-to-noise (S/N) ratio (V_{in} = 10mV)	58dB
Intermodulation distortion	–55dB
A.F.C. sensitivity	10V/100kHz
Video output signal	3V
Input sensitivity into 2kΩ (onset of a.g.c.)	100μV e.m.f.

PRACTICAL R.F. AND I.F. CIRCUITS

Both the practical circuits described in Ref.1 are suitable for the TDA2540 or TDA2541, and provide operation on the UK System I or the Continental System B/G. In the first circuit, i.f. selectivity is provided by a conventional LC filter, and in the second circuit a recently-introduced surface-wave filter provides the selectivity. The preamplifier for the surface-wave filter has provision for either double-tuned or single-tuned coupling.

Details are given in Ref.1 of the main printed-wiring board and subsidiary boards. The main board can accommodate either practical circuit, and has provision for a sound channel module and a video filter module. (These modules are not described in Ref.1.)

Fig.2 shows the main board containing the U321 u.h.f. tuner, SW102/M surface-wave filter, and TDA2540 IC. The module comprising the surface-wave filter and preamplifier is shown with the screening cover removed.

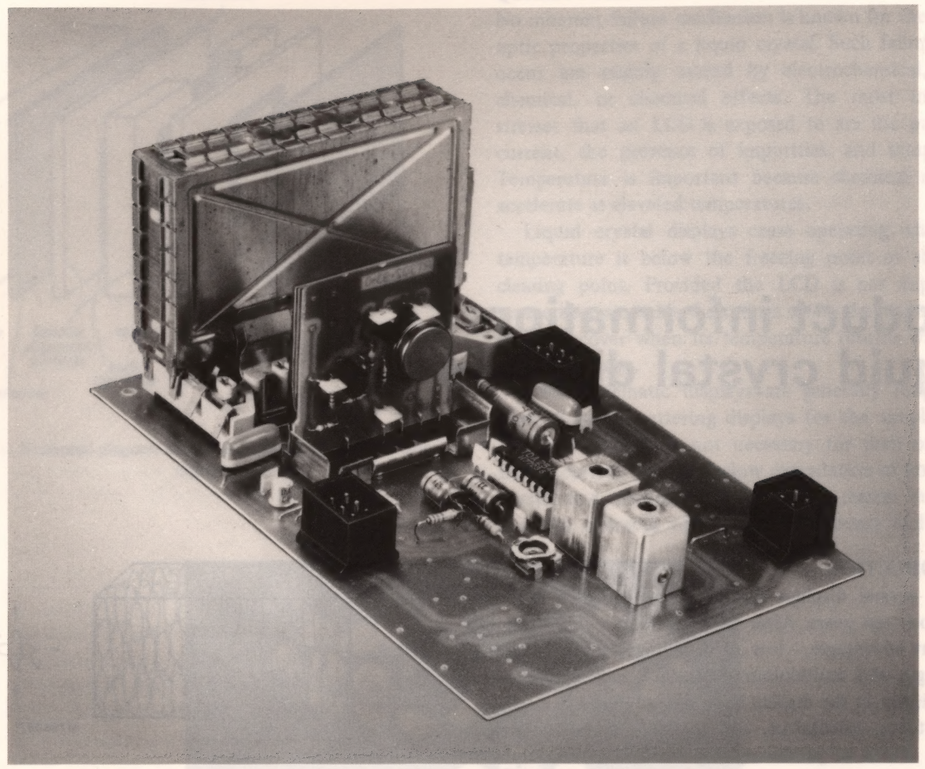


Fig.2 – Board containing the U321 u.h.f. tuner, SW102/M surface-wave filter, and TDA2540 IC

REFERENCE

1. BECKLEY, J.C., MASON, M.E., and ROSE, M.A., 'TDA2540 and TDA2541: vision-i.f. integrated circuits', Technical Information 71, TP1675, Mullard Limited, 1978.

Product information: Liquid crystal displays

INTRODUCTION

Liquid crystal displays (LCDs) have now been around for about ten years. After early teething troubles, their inherent advantages – low drive voltage, great freedom of design, and multicolour potential – have established them firmly in the display field. Already used in electronic watches, calculators, and digital instruments, they offer a means of producing large-screen flat thin alpha-numeric and pictorial displays.

Liquid crystal displays are passive devices. They rely on external light sources, and their readability is largely determined by the method of illumination. Since LCDs do not produce light but modulate incident light, their power consumption is small, making them suitable for direct drive from ICs.

Detailed information on LCDs is given in Ref.1, which is available on request.

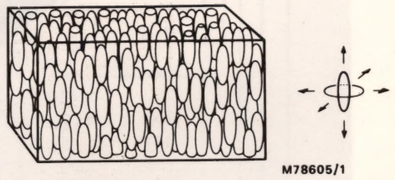


Fig.1 — Molecular arrangements in a nematic liquid crystal and their freedom of movement

LIQUID CRYSTALS

Certain substances can exist in a state in which they exhibit properties of both solids and liquids. These substances are called liquid crystals. Like liquids, they are fluid and their molecules have a large freedom of movement; however, as with crystalline solids, their molecules retain a degree of ordering. Generally they remain oriented in a preferred direction, but are free to interchange positions or rotate around their long axes. (See, for example, Fig.1.)

This partially-ordered liquid-crystal state exists between sharply defined transition temperatures: the solid-liquid transition, melting point, and a higher temperature above which the liquid becomes completely disordered, the clearing point T_c. Between these two temperatures, the molecular axes have a preferred orientation known as the director of the liquid crystal.

Liquid crystals exhibit electro-optic effects several orders of magnitude larger than those previously known.

LIQUID CRYSTAL DISPLAYS

A cell, consisting of two conducting glass plates sandwiching a thin layer of liquid crystal, forms a liquid crystal electro-optic device. These cells are used in two different modes: transmissive, where light is transmitted through the cell, and reflective, where the incident light is reflected back at the observer by the back electrode – a reflecting aluminium film on a glass substrate. The front electrode only is transparent for the reflective cell, but for the transmissive cell both electrodes are transparent.

The construction of a cell using a twisted-nematic liquid crystal is shown in Fig.2, and an example of such cells used in a clock face is shown in Fig.3.

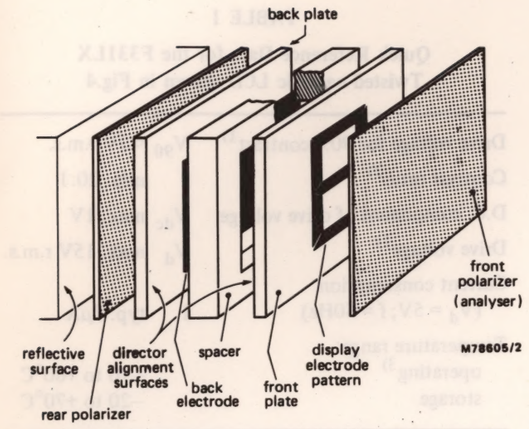


Fig.2 — Exploded diagram of an LCD using a twisted-nematic liquid crystal

QUALITY ASPECTS

No inherent failure mechanism is known for the electro-optic properties of a liquid crystal. Such failures as do occur are mainly caused by electrochemical, photochemical, or chemical effects. The most important stresses that an LCD is exposed to are the passage of current, the presence of impurities, and temperature. Temperature is important because chemical reactions accelerate at elevated temperatures.

Liquid crystal displays cease operating when their temperature is below the freezing point or above the clearing point. Provided the LCD is not exposed to temperatures outside the ratings set by the manufacturer, it will recover when its temperature returns within the operating range.

Twisted-nematic displays are generally longer lived than dynamic-scattering displays for the simple reason that current-flow is not necessary for their operation. Direct current can cause slow degradation of both liquid crystal and electrodes. It is for this reason that LCDs must be operated with a.c. at a frequency high enough

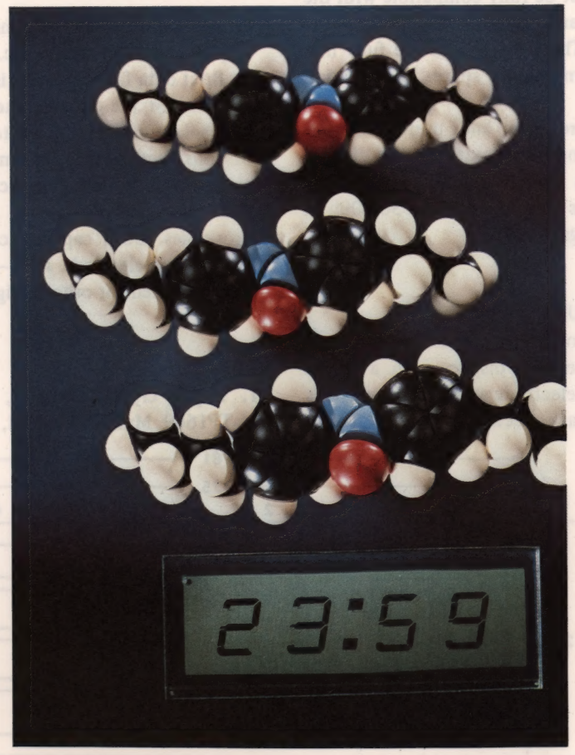


Fig.3 — Liquid crystal clock display (type F331LX) and three models of liquid-crystal molecules in their natural parallel orientation. The models are of p-p′-n dibutyl azoxy molecules (often known as DIBAB). The butyl groups are shown coloured black and white, the azoxy (bridging) groups are blue and red

to avoid electrode polarisation. Extra protection is afforded by the d.c.-blocking layer applied to the electrodes.

Other possible causes of liquid-crystal degradation are ultraviolet light, the presence of reactive impurities, and the action of air or water.

Most incident ultraviolet light is absorbed by the glass cell walls and light-modulation foils. Ionic impurities are excluded by cleanliness in assembly, and the proper selection and preparation of materials. Where the liquid crystal is air-sensitive or water-sensitive, it is important that these be rigorously excluded during the filling and sealing of the cell, and that the cell is hermetically sealed.

The sensitivity of an LCD to light, impurities, and moisture depends to a large extent on the type of liquid crystal used, which in turn depends on the available display-construction technology.

The director-orienting layer is an important factor in determining the useful life of a display. It should not dissolve in, or be otherwise affected by, the liquid crystal. Moreover, it should not absorb impurities. The orientation technique must be fully compatible with the cell sealing procedure and should not impair the hermeticity of the cell. These conditions are fully met by the polymer film-thermoplastic spacer combination used.

Naturally, both failure rate and useful life are dependent on the size and complexity of the display. Twisted-nematic displays of normal size ($\simeq 50cm^2$) generally have useful lives well in excess of 30 000h at maximum permitted ratings.

TABLE 1

Quick Reference Data for the F331LX Twisted-nematic LCD shown in Fig.4

Drive voltage for 90% contrast[1]	V_{90}	<3V r.m.s.
Contrast ratio[2]		min. 20:1
D.C. component of drive voltage	V_{dc}	max. 1V
Drive voltage[1]	V_d	max. 15V r.m.s.
Current consumption (V_d = 5V; f = 50Hz)	I	typ. 5μA
Temperature range:		
operating[3]		−10 to +60°C
storage		−20 to +70°C

Notes:
1. Squarewave drive.
2. Measured in transmission and normal to the display surface.
3. Can be supplied for other limits using a different blend of crystal.

elements are brought to connection pads separately. The display is protected by a d.c.-blocking layer.

Brief data for the device is given in Table 1.

Some of the data for the LCD applies to this design of display only, and some to all displays using this type of construction and the same liquid crystal. All voltage and frequency characteristics are independent of display size and electrode area, as are the electro-optical properties. Both capacitance and current consumption depend on electrode area – $2.5cm^2$ in this case – and may be scaled for other designs.

PROPERTIES OF PRODUCTION DISPLAYS

Fig.4 shows a standard production digital-clock LCD. It is a field-effect twisted-nematic display with a visible area of $18cm^2$ and a total electrode area of $2.5cm^2$. This display has a common back electrode, and all display

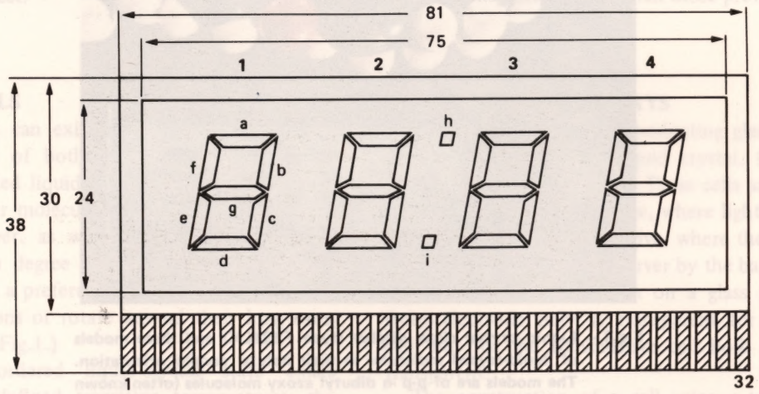


Fig.4 – Standard, 4-digit twisted-nematic clock LCD type F331LX

REFERENCE

1. 'Liquid crystal displays', Technical Information 69, TP1669, Mullard Limited, 1978.